MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-A

User's Manual

type A3HCPU

UAHP

MITSUBISHI ELECTRIC

REVISIONS

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum.
A copy of this manual should be forwarded to the end User.

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1. INTRODUCTION

This manual includes specifications, functions, and handling instructions for the A3HCPU general-purpose programmable controller.

The A3HCPU is a high speed PC for use with standard A-Series I/O modules and the majority of the A-Series special function modules. It is programmed in the same way as the other A-Series CPUs with some minor changes.

1.1 How to Use This Manual.

This manual is divided up into sections as follows:

Section 2:	Compatibility of programming peripherals, special function units and utility software packages. General information on system configurations.
Section 3:	Hardware, software and performance specifications. Definitions and explanations of A3HCPU software features.
Section 4:	Nomenclatures for A3HCPU and associated hardware. Hardware preparation, switch setting etc.
Section 5:	Installation instructions, environmental considerations, power supply requirements etc.
Section 6:	Pre-start-up test and check procedures.
Section 7:	Troubleshooting. List and definitions of error codes. Troubleshooting digital I/O wiring.
Section 8:	Periodic maintenance and inspection requirements. Battery and fuse replacement.
Appendices	

The following manuals may also be required

A1(E), A2(E), A3(E) CPU I/O unit user's manual
A1(E), A2(E), A3(E) CPU Programming manual
A3HCPU P21/R21 Data Link Unit User's Manual
Data Link Unit User's Manual

In this manual the A6GPP, A6PHP and A6HGP are referred to as GPP/PHP/HGP respectively.

1.2 Comparison between A3HCPU and A1(E), A2(E), A3(E) CPUs

Item \ Type		A3HCPU	A1(E)CPU	A2(E)CPU	A3(E)CPU
Control method		Stored program, repeated operation	Stored program, repeated operation		
I/O control mode		Refresh/direct (selectable)	A1, A2, A3CPUs direct A1E, A2E, A3ECPUs refresh		
Programming language		Language dedicated to sequence control (Relay symbol, logic symbolic language)	Language dedicated to sequence control (Relay symbol, logic symbolic language)		
Use with MELSAP language		No	Yes		
Number of instructions	Sequence instruction	22 types	22 types		
	Basic instruction	132 types	131 types		132 types
	Application instruction	107 types	99 types	103 types	107 types
Processing speed (Sequence instruction)		Direct mode: 0.2 to 2 μS/step Refresh mode: 0.2 to 0.4 μS/step	1.25 to 2.25 μS/step		
Number of I/O points		2048	256	512	2048
Constant scan function (Program start at specified intervals)		Can be set between 10 and 190ms in 10ms increments.	A3ECPU only		
Watch dog timer (WDT)		200ms only	Can be set between 10 and 2000ms in 10ms increments.		
Allowable instantaneous power failure		Within 20ms	Within 20ms		
Current consumption (A)		3	1.5	1.6	1.7
Size mm (inches)		250 (9.84) x 79.5 (3.13) x 121 (4.76)	250 (9.84) x 135 (5.32) x 121 (4.76)	250 (9.84) x 79.5 (3.13) x 121 (4.76)	
Weight kg (lb)		0.9 (1.98)	1.65 (3.63)	0.7 (1.54)	0.8 (1.76)
Memory capacity		Max. 144K bytes	Max. 16K bytes	Max. 144K bytes	
Program capacity	Main sequence program	Max. 30K steps	Max. 6K steps	Max. 14K steps	Max. 30K bytes
	Subsequence program	Max. 30K steps	Unavailable		Max. 30K steps
	Microcomputer program	Max. 58K bytes	Max. 10K bytes	Max. 26K bytes	Max. 58K bytes
Internal relay (M)		1000 points (M0 to 999) — A total of 2048 points may be defined as M, L or S in the parameters	1000 points (M0 to 999) — A total of 2048 points may be defined as M, L or S in the parameters		
Latch relay (L)		1024 points (L1000 to 2047)	1024 points (L1000 to 2047)		
Step relay (S)		0 point (defaults to no value)	Unavailable		
Link relay (B)		1024 points (B0 to 3FF)	1024 points (B0 to 3FF)		
Timer (T)	Number of points	256	256		
	Specifications	100ms timer: set time 0.1 to 3276.7 sec (T0 to 199) 10ms timer: set time 0.01 to 327.67 sec (T200 to 255) 100ms retentive timer: set time 0.1 to 3276.7 sec — Set in parameters			
Counter (C)	Number of points	256	256		
	Specifications	Normal counter: set value 1 to 32767 (C0 to 255) Interrupt counter: set value 1 to 32767 (C224 to C255 user specified) Counts the number of interrupt signals received.	Normal counter: set value 1 to 32767 (C0 to 255) — Set in parameters Interrupt program counter: set value 1 to 32767 Counter used in interrupt program		
Data register (D)		1024 points (D0 to 1023)	1024 points (D0 to 1023)		
Link register (W)		1024 points (W0 to 3FF)	1024 points (W0 to 3FF)		
Annunciator (F)		256 points (F0 to 255)	256 points (F0 to 255)		

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Item \ Type	A3HCPU	A1(E)CPU	A2(E)CPU	A3(E)CPU
File register (R)	Max. 8192 points (R0 to 8191)	Unavailable	Max. 4096 points (R0 to 4095)	Max. 8192 points (R0 to 8191)
Accumulator (A)	2 points (A0, A1)	2 points (A0, A1)		
Index register (V, Z)	2 points (V, Z)	2 points (V, Z)		
Pointer (P)	256 points (P0 to 255)	256 points (P0 to 255)		
Interrupt pointer (I)	32 points (I0 to 31)	32 points (I0 to 31)		
Special relay (M)	256 points (M9000 to 9255)	256 points (M9000 to 9255)		
Special register (D)	256 points (D9000 to 9255)	256 points (D9000 to 9255)		
Number of comments	Max. 4032	128 (for F0 to 127 only)	Max. 4032 points	
Status latch function	Available	Unavailable	Available	
Sampling trace function	Available	Unavailable	Available	
Offline switch function	Unavailable	Available (Y, M, L, B, F)		
Annunciator display function	F number indication	Unavailable		F number indication
Remote run/pause contact setting	Available	Available		
Operation mode switching during error occurrence	Available	Available		
Output mode switching at change from STOP to RUN	Available	Available		
Entry code	Available	Available		
Print title entry	Available	Available		
Software I/O assignment	Using GPP/ PHP/HGP	Using GPP/PHP/HGP		

2.2 System Equipment

Key: M: Master
L: Local
R: Remote
O: Applicable

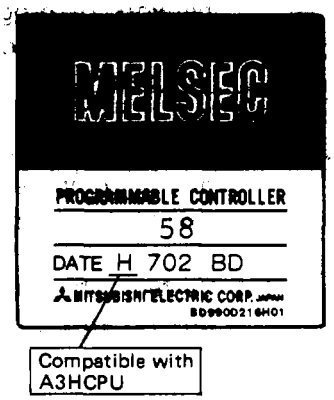
Unit		Type	Description	Occupied Points	Applicable System								Remarks
					Independent	Coaxial data link			Optical data link			Computer link	
						M station	L station	R station	M station	L station	R station		
CPU unit		A3HCPU	Program capacity: 30K steps, I/O points: 2048 points M, L total: 2048 points, T: 256 points C: 256 points, D: 1024 points	—	O	—	—	—	—	—	—	O	Memory cassette to be arranged separately.
		A3HCPUR21	For coaxial data link (Master, local selectable)		O	O	O	—	—	—	—	O	
		A3HCPUP21	For optical data link (Master, local selectable)		O	—	—	—	O	O	—	O	
Memory cassette		A3MCA-0	Without IC-RAM memory	—	O	O	O	—	O	O	—	O	• With two memory sockets •A3MAC-0 can be loaded with IC-RAM or EP-ROM memory. •A3MCA-2 to -18 can be loaded with only EP-ROM memory.
		A3MCA-2	With IC-RAM memory 16K bytes (max. 6K steps)										
		A3MCA-4	With IC-RAM memory 32K bytes (max. 14K steps)										
		A3MCA-8	With IC-RAM memory 64K bytes (max. 30K steps)										
		A3MCA-12	With IC-RAM memory 96K bytes (max. 46K steps)										
		A3MCA-18	With IC-RAM memory 144K bytes (max. 60K steps)										
Memory	IC-RAM	*4KRAM	8K bytes (max. 3K steps)	—	O	O	O	—	O	O	—	O	
	EP-ROM	*4KROM	8K bytes (max. 3K steps)										
		8KROM	16K bytes (max. 7K steps)										
		16KROM	32K bytes (max. 15K steps)										

Table 2.1 List of Equipment

2.2.1 Notes on compatibility with other MELSEC-A series equipment

1) All digital I/O modules are compatible with the A3HCPU.
2) All special function units (including analog I/O modules) are compatible with the A3HCPU with the following exceptions:

a)	AJ71C23	Incompatible.
b)	AD57	Incompatible.
c)	AD58	Incompatible.
d)	AJ71C24	Versions with H preceding the serial number, as shown below, are compatible.
e)	AD51	Versions with H preceding the serial number, as shown below, are compatible.

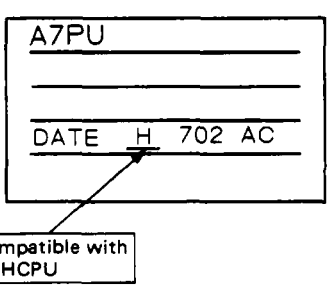


3) The following microcomputer software packages are incompatible with the A3HCPU:

a)	SWOC-UTLP-PID	Incompatible.
b)	SWOC-UTLP-FNO	Incompatible.
c)	SWO-AD57P	Incompatible.

4) The following restrictions apply to the use of peripheral programming equipment with the A3HCPU:

a)	A6GPP/A6PHP	Use software package SW3GP-GPPA□□-1/2, or subsequent versions.
b)	A6HGP	Use software package SW3-HGPA□□-1/2, or subsequent versions.
c)	A7PU	Versions with H preceding the serial number, as shown below, are compatible.
d)	A6WU	Versions with H preceding the serial number, as shown below, are compatible.



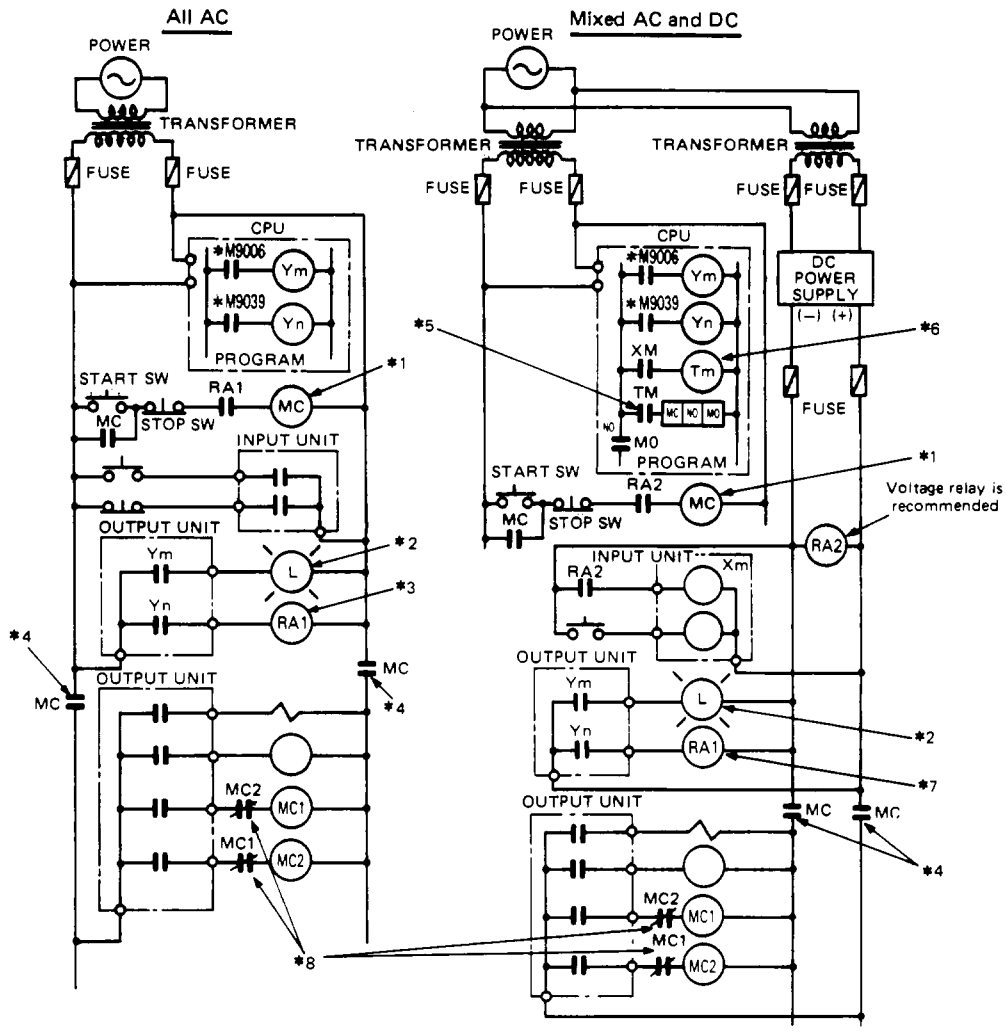
2.4 System Design Considerations

This section gives advice on the design of the control system for use with the A3HCPU.

2.4.1 Safety circuit

Note the following:
On switching on the PC power supply, there is a short but finite time before the DC levels reach their operating values. During this period, the unit will not operate normally. The same applies when the power is cut as the DC levels drop below their operating values. The following circuit will overcome any problems which may arise in output control due to this phenomenon.

System design circuit example



**1: Run/stop circuit interlocked with RA1 (run monitor relay)*
**2: Battery low alarm*
**3: RA1 switched on by M9039 (run monitor relay)*
**4: Power to output equipment switched off when stop signal given.*
**5: Input switched when power supply established.*
**6: Set time for DC power supply to be established.*
**7: On when run by M9039*
**8: Interlock circuit as neccessary.*

The power-on procedure is as follows:

For AC

1) Switch on power.
2) Set CPU to RUN.
3) Switch on the start switch.
4) When the magnetic contactor (MC) comes in, output equipment is powered and may be driven from the program.

For AC/DC

1) Switch on power.
2) Set CPU to RUN.
3) When DC power is established, RA2 turns on.
4) Timer (TM) times out after the DC power reaches 100%.
   (The set value of TM should be the period of time from when RA2 switches on to the establishment of 100% DC voltage. Set the set value to approximately 0.5 seconds.)
5) Switch on the start switch.
6) When the magnetic contactor (MC) comes in, the output equipment is powered and may be driven by the program.

2.4.2 Unit selection

(1) Power supply unit

(a) Select the power supply according to the 5V DC current required in the system.
If the capacity is too small, there will be a drop in the DC 5V, resulting in CPU shutdown, erroneous I/O signals, etc.

(b) The 5V DC power to an A55B or A58B extension base, is supplied from the power supply on the main base unit. When using either of these extension bases ensure that the power supply selected has sufficient capacity for both bases.

(c) When using the 24V DC output from the power supply ensure that the current capacity is never exceeded.

(d) When using an A66P power supply unit, install it at the right end of the base unit.
The unit located to the left of the A66P must be selected according to Section 3.3.2 (3) as the 24V DC output from the A66P varies according to this unit.

(e) Power supply specifications can be found in Section 3.3.

(2) Extension base unit

For base units (A55B, A58B) not requiring their own power supply unit, 5V DC is supplied from the power supply unit in the main base unit via the extension cable, as described in (2) (a) above. In this case, a voltage drop occurs over the extension cable so that the voltage at the receiving end is less than that at the source end.
Since at least 4.75V DC is required at the receiving end, it is neccessary to select the base unit so that the voltage does not drop to less than 4.75V DC. For information on selecting the A55B or A58B, refer to Section 3.4.3.

REMARKS

For information on I/O units, refer to the A1, A2, A3CPU I/O Unit User's Manual.

3. SPECIFICATIONS

3.1 General Specifications

Item	Specifications				
Operating ambient temperature	0 to 55°C				
Storage ambient temperature	−10 to 75°C				
Operating ambient humidity	10 to 90%RH, non-condensing				
Storage ambient humidity	10 to 90%RH, non-condensing				
Vibration resistance	Conforms to JIS C 0911	Frequency	Acceleration	Amplitude	Sweep Count
		10 to 55Hz	−	0.075mm	10 times *(1 octave/minute)
		55 to 150Hz	1g	−	
Shock resistance	Conforms to JIS C 0912 (10g x 3 times in 3 directions)				
Noise durability	By noise simulator of 1000Vpp noise voltage, 1μs noise width and 25 to 60Hz noise frequency				
Dielectric withstand voltage	1500V AC for 1 minute across AC external terminals and ground 500V AC for 1 minute across DC external terminals and ground				
Insulation resistance	5MΩ or larger by 500V DC insulation resistance tester across AC external terminals and ground				
Grounding	Class 3 grounding (Grounding not neccessary for PC operation)				
Operating ambience	Free of corrosive gases. Dust should be minimal.				
Cooling method	Self-cooling				

Table 3.1 General Specifications

REMARKS

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10Hz to 20Hz, from 20Hz to 40Hz, from 40Hz to 20Hz, and 20Hz to 10Hz are referred to as one octave.

3.2 A3HCPU Unit Performance Specifications

3.2.1 A3HCPU unit performance specifications

Items marked ★ in the table are enabled, or their ranges assigned, in the PC parameters using the peripheral equipment (PU, GPP, PHP or HGP, but partly restricted in the case of PU). For details of parameter setting, refer to Section 3.2.8 "Parameter and range setting". The following table shows default settings:

Item		Performance
Control system		Stored program, repeated operation
I/O control method (I/O control setting)		Direct/refresh method
Programming language		Language dedicated to sequence control (Combined use of relay symbol type, logic symbolic language)
Instruction	Sequence instruction	22 types
	Basic instruction	132 types
	Application instruction	107 types
Processing speed	Direct mode	Sequence instruction 0.2 to 2 μs/step
	Refresh mode	Sequence instruction 0.2 to 0.4 μs/step
Constant scan (program start at specified intervals)		Can be set between 10ms and 190ms in 10ms increments
Memory capacity and memory type	Memory capacity	Max. 144K bytes
	Memory type (Memory cassette type)	Memory cassette A3MCA-0 to A3MCA-18 (For memory cassette details, refer to Section 3.8.)
★ Main sequence program capacity		6K steps (Can be set to max. 30K steps)
I/O points		2048 points
★ Internal relay (M)		1000 points (1000 bits)
★ Latch relay (L)		1048 points (1048 bits)
★ Step relay (S)		Defaults to no value. Used in the same manner as the internal relays
		The number of M+L+S devices is 2048
Link relay (B)		B0 to 3FF 1024 points (1024 bits)

Table 3.2 Performance Specifications

Item		Performance
★ Timer	Number of points	256 points
	Specifications	T0 to 199, 100ms timer: setting time 0.1 to 3276.7 sec T200 to 255, 10ms timer: setting time 0.01 to 327.67 sec 100ms retentive timer: depending on setting (setting time 0.1 to 3276.7 sec) ○Set values can be changed by parameters. ○Timer accuracy +2 scan times −1 scan time
★ Counter	Number of points	256 points
	Specifications	C0 to 255, normal counter: setting range 1 to 32767 (C224 to C255 may be used as interrupt counters. See Section 3.2.15.)
Data register (D)		D0 to 1023, 1024 points (16 bits per word)
Link register (W)		W0 to 3FF, 1024 points (16 bits per word)
Annunciator (F)		F0 to 255, 256 points (256 bits)
★ File register (R)		Depending on setting (Max. 8192 points)
Accumulator (A)		A0, A1, 2 points (2 words)
Index register (V, Z)		V, Z, 2 points (2 words)
Pointer (P)		P0 to 255, 256 points
Pointer for interruption (I)		I0 to 31, 32 points
Special relay (M)		M9000 to 9255, 256 points (256 bits)
Special register (D)		D9000 to 9255, 256 points (256 words)
★ Status latch		Set in parameters (Max. 24K bytes)
★ Sampling trace		Set in parameters (Yes. . . . .8K bytes)
★ Comment		Set in parameters (Max. 4032 points)
★ Subsequence program capacity		Set in parameters (Max. 30K steps)
★ Latch (power failure compensation) range		L1000 to L2047 (1048 points)
★ Link range		Set in parameters
★ Remote run/pause contact		Set in parameters
★ Operation mode at the time of error		I/O error : STOP Software instruction error : CONTINUE
★ Annunciator display mode		F number display
★ STOP → RUN output mode		Output data at time of STOP is restored.
★ Entry code		Set in parameters
★ Print title entry		Set in parameters

Table 3.2 Performance Specifications (Continued)

Item		Performance
★ I/O assignment		The number of I/O points allocated to each slot is dictated by the individual I/O units used. An empty slot occupies 16 points. For details, refer to Section 3.2.22.
★ Self-diagnostic functions		Watch dog error monitor (watch dog timer 200ms only) Memory error detection, CPU error detection, I/O error detection, battery error detection, etc. (For details, refer to Section 3.2.7.)
At power-on, at power restoration after power failure		Automatic restart when "RUN" switch is moved to ON position (Initial start)
IC-RAM backup		By lithium battery Battery guaranteed for 5 years. For total power failure guarantee time, refer to Section 8.3.
Parameters		Items marked ★ in this table are set in parameter mode using any of the peripheral programming devices.
Other functions	Step run	Break point setting and run per instruction can be executed using peripheral equipment (not PU) connected to the CPU unit.
	Interrupt processing	Interrupt program can be run in response to a signal from an interrupt unit or by a constant-cycle interrupt signal.
	Data link	Data link system incorporating local PCs and/or remote I/O can be constructed.
	★ Microcomputer mode	Depending on setting
Allowable instantaneous power failure time		Within 20ms
Current consumption (A)		3.0
Weight kg (lb)		0.9 (1.98)
External dimensions mm (inches)		250 x 79.5 x 121 (9.84) (3.13) (4.76)

Table 3.2 Performance Specifications

POINT

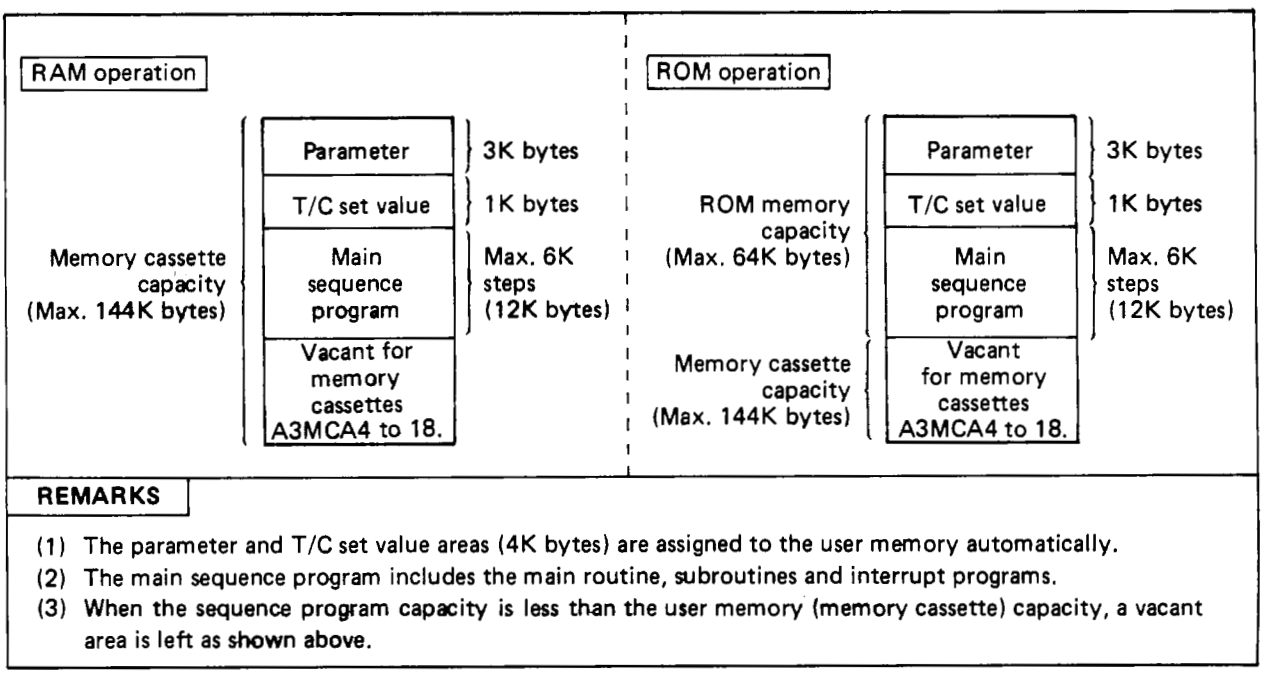
MELSAP (MELSEC Flow diagram programming language) cannot be used to write A3HCPU programs.

3.2.2 User memory assignment

The user memory may be arranged as required to suit the individual application. Memory allocation is made using any of the peripheral programming devices. Where memory allocation has not been made, the PC uses its default settings as described in paragraph (1) below.

(1) User memory not assigned by parameter setting.

The following memory maps are the default settings adopted by the PC when parameter setting has not been made.



REMARKS

(1) The parameter and T/C set value areas (4K bytes) are assigned to the user memory automatically.
(2) The main sequence program includes the main routine, subroutines and interrupt programs.
(3) When the sequence program capacity is less than the user memory (memory cassette) capacity, a vacant area is left as shown above.

(2) User memory assigned in parameters.

In order to enable some of the PC functions, memory areas must be allocated according to the function required using any of the peripheral programming devices (use of the PU, however, is limited). Memory areas to which allocation may be made are shown below. Note that the total amount of memory used must not be greater than the capacity of the memory cassette used.

RAM operation

Memory cassette RAM area

Parameter	4K bytes are always required from the user memory area for storing the parameter settings.
T/C set value	
Sequence program	Can be set between 1 and 30K steps (2 and 60K bytes) in 1K step (2K byte) increments.
Microcomputer program	
Sampling trace	No (0K byte) or yes (8K bytes) can be selected.
Status latch – Data area	No (0K byte) or yes (8K bytes) can be selected.
Status latch – File register	No (0K byte) or yes (bytes set for file registers) can be selected.
File register	Can be set between 0 and 16K bytes (0 and 8192 points) in 2K byte (1024 point) increments.
Comment	Can be set between 0 and 64K bytes (0 and 4032 points) in 1K byte (64 point) increments.

ROM operation

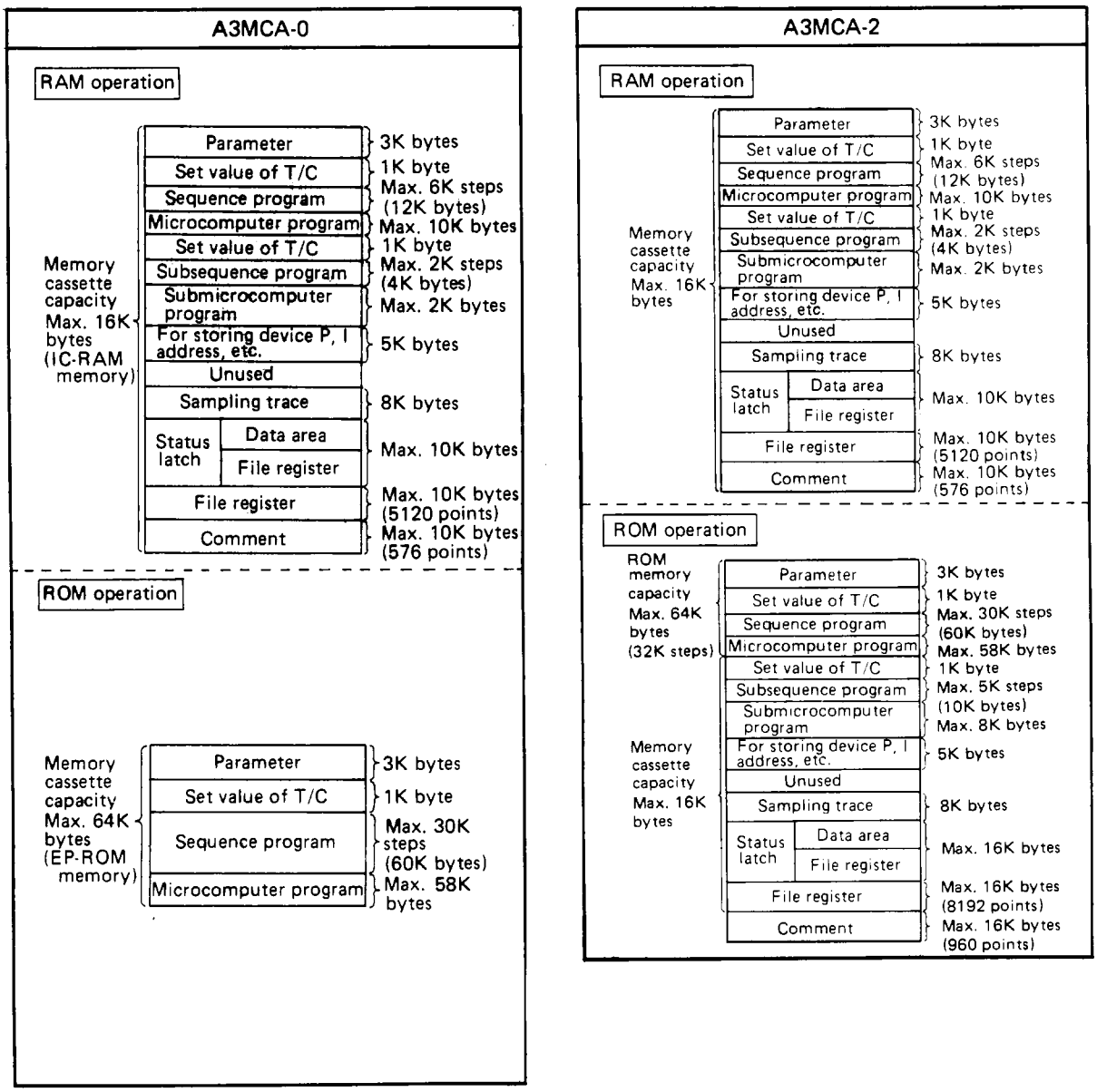
Memory cassette ROM area

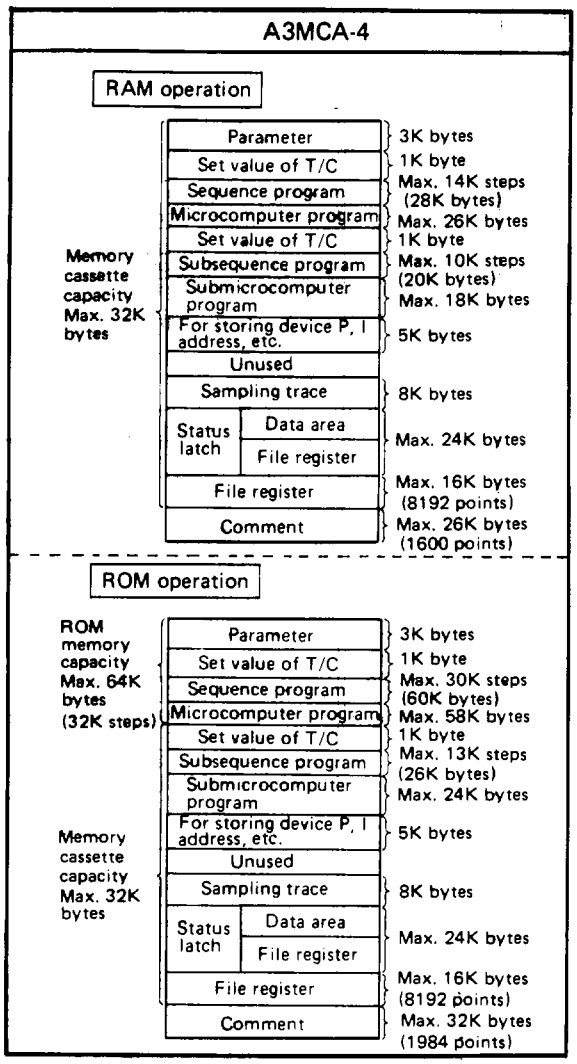
Parameter	4K bytes are always required from the user memory area for storing the parameter settings.
T/C set value	
Sequence program	Can be set between 1 and 30K steps (2 and 60K bytes) in 1K step (2K byte) increments.
Microcomputer program	

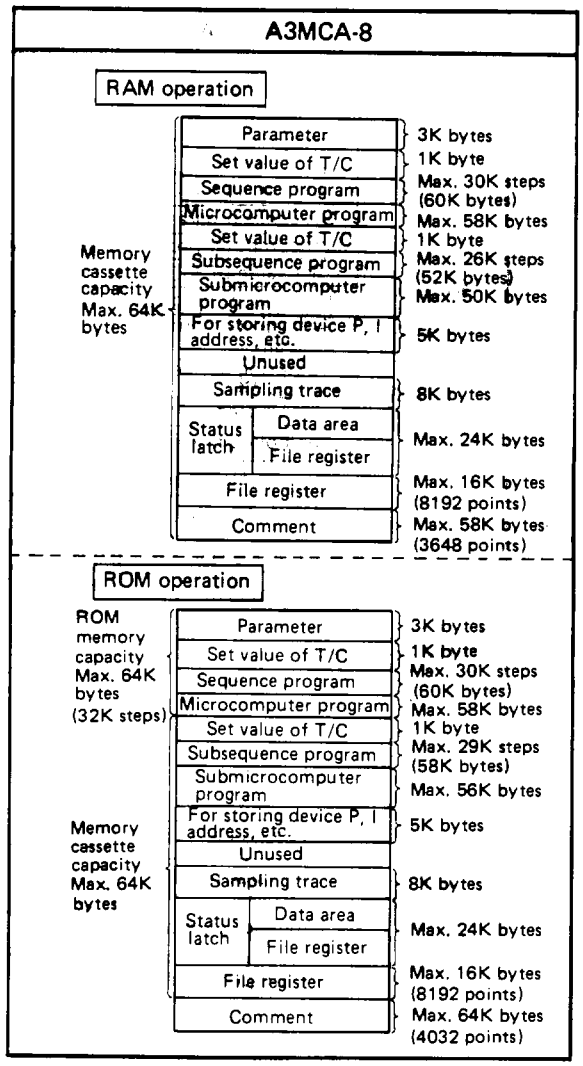
Memory cassette RAM area

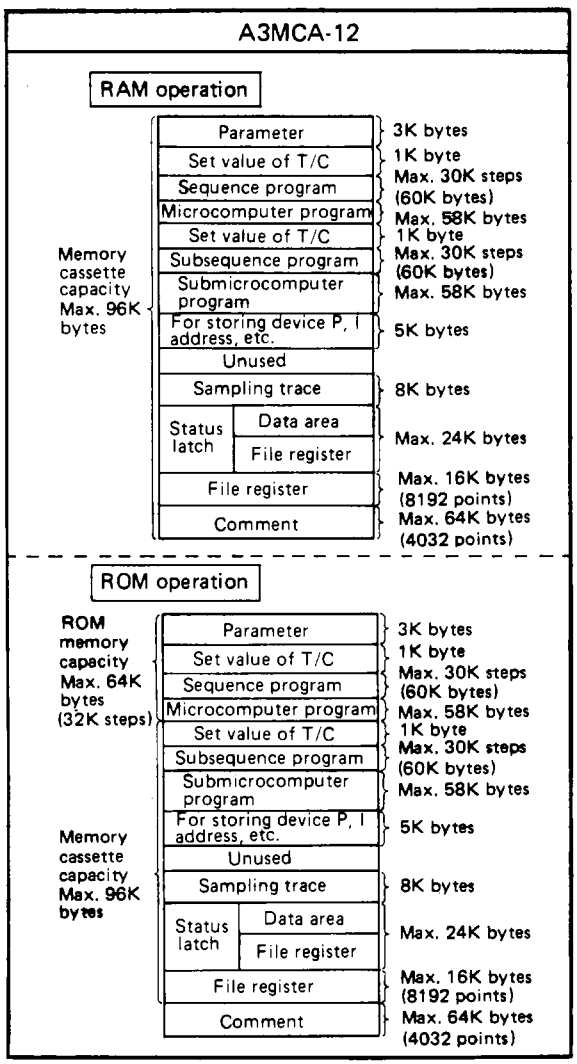
Sampling trace	No (0K byte) or yes (8K bytes) can be selected.
Status latch – Data area	No (0K byte) or yes (8K bytes) can be selected.
Status latch – File register	No (0K byte) or yes (bytes set for file registers) can be selected.
File register	Can be set between 0 and 16K bytes (0 and 8192 points) in 2K byte (1024 point) increments.
Comment	Can be set between 0 and 64K bytes (0 and 4032 points) in 1K byte (64 point) increments.

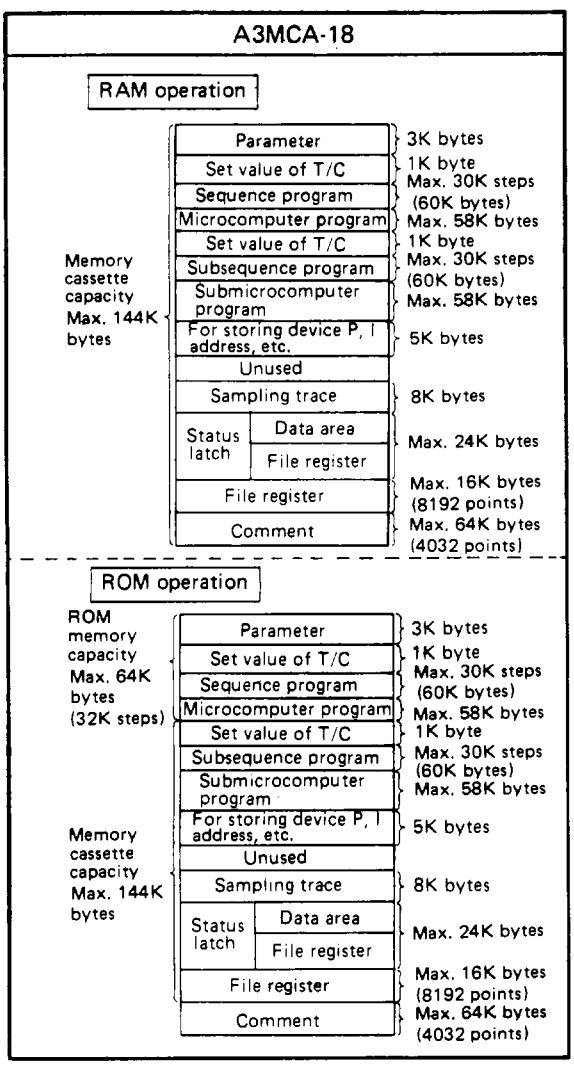
The A3HCPU memory may be assigned within the following ranges depending on the memory cassette used.




A3MCA-4
RAM operation
Memory cassette capacity Max. 32K bytes
Parameter 3K bytes
Set value of T/C 1K byte
Sequence program Max. 14K steps (28K bytes)
Microcomputer program Max. 26K bytes
Set value of T/C 1K byte
Subsequence program Max. 10K steps (20K bytes)
Submicrocomputer program Max. 18K bytes
For storing device P, I address, etc. 5K bytes
Unused
Sampling trace 8K bytes
Status latch
Data area
File register
Max. 24K bytes
File register Max. 16K bytes (8192 points)
Comment Max. 26K bytes (1600 points)
ROM operation
ROM memory capacity Max. 64K bytes (32K steps)
Parameter 3K bytes
Set value of T/C 1K byte
Sequence program Max. 30K steps (60K bytes)
Microcomputer program Max. 58K bytes
Set value of T/C 1K byte
Subsequence program Max. 13K steps (26K bytes)
Submicrocomputer program Max. 24K bytes
Memory cassette capacity Max. 32K bytes
For storing device P, I address, etc. 5K bytes
Unused
Sampling trace 8K bytes
Status latch
Data area
File register
Max. 24K bytes
File register Max. 16K bytes (8192 points)
Comment Max. 32K bytes (1984 points)


A3MCA-8
RAM operation
Memory cassette capacity Max. 64K bytes
Parameter 3K bytes
Set value of T/C 1K byte
Sequence program Max. 30K steps (60K bytes)
Microcomputer program Max. 58K bytes
Set value of T/C 1K byte
Subsequence program Max. 26K steps (52K bytes)
Submicrocomputer program Max. 50K bytes
For storing device P, I address, etc. 5K bytes
Unused
Sampling trace 8K bytes
Status latch
Data area
File register
Max. 24K bytes
File register Max. 16K bytes (8192 points)
Comment Max. 58K bytes (3648 points)
ROM operation
ROM memory capacity Max. 64K bytes (32K steps)
Parameter 3K bytes
Set value of T/C 1K byte
Sequence program Max. 30K steps (60K bytes)
Microcomputer program Max. 58K bytes
Set value of T/C 1K byte
Subsequence program Max. 29K steps (58K bytes)
Submicrocomputer program Max. 56K bytes
Memory cassette capacity Max. 64K bytes
For storing device P, I address, etc. 5K bytes
Unused
Sampling trace 8K bytes
Status latch
Data area
File register
Max. 24K bytes
File register Max. 16K bytes (8192 points)
Comment Max. 64K bytes (4032 points)





REMARKS

(1) 4K bytes of user memory are always required for parameter and timer/counter set value storage.
(2) "sequence program" includes subroutine and interrupt programs.
(3) Note the following when assigning memory protect areas:
Parameter, sequence program and subsequence program areas are assigned, in order, to the beginning of the memory map.
Comment, file register, status latch, and sampling trace areas are assigned to the end of the memory map as indicated above. There is therefore an unused memory range between the two areas. Memory protect should therefore be assigned to the first part of the memory map.
(4) The maximum values for items shown above indicate the maximum value for that item taken on its own.
(5) When mixing ROM and RAM, any item other than the sequence program may be assigned to RAM.
(6) The capacities shown above for microcomputer and submicrocomputer programs are the maximum possible with the corresponding sequence program area set to 1K steps (=2K bytes). Sequence program + microcomputer program must be $\leqslant$ 60K bytes.

3.2.3 Device list

This section gives the names and address ranges of the devices available on the A3HCPU. Items marked* in the table are enabled, or their ranges assigned, in the PC parameters using the peripheral equipment (PU, GPP, PHP or HGP, but partly restricted in the case of PU). For details of parameter setting, see Section 3.2.8 "Parameter and range setting."

	Device		Points	Remarks
	X	Input	X, Y0 to 7FF (X, Y total 2048 points)	X, Y numbers are in hexadecimal
	Y	Output		
	M	Special relay	M9000 to 9255 (256 points)	
*		Internal relay	M0 to 999 (1000 points) — Total number of devices M+L+S=2048	
*	L	Latch relay	L1000 to 1024 (1024 points)	
*	S	Step relay	Set in parameters (0 point)	
	F	Annunciator	F0 to 255 (256 points)	
*	T	100ms timer	T0 to 199 (200 points)	There are 256 points of timers and counters, respectively.
		10ms timer	T200 to 255 (56 points)	
		100ms retentive timer	Set in parameters (0 point)	
*	C	Counter	C0 to 255 (256 points)	
		Interrupt counter	Set in parameters (0 point)	
	D	Data register	D0 to 1023 (1024 points)	
		Special register	D9000 to 9255 (256 point)	
	W	Link register	W0 to 3FF (1024 points)	W numbers are in hexadecimal
•	R	File register	Set in parameters (0 point)	
	A	Accumulator	A0, A1 (2 points)	
	Z	Index register	Z (1 point)	
	V		V (1 point)	
	N	Nesting	N0 to 7 (8 levels)	
	P	Pointer	P0 to 255 (256 points)	
	I	Pointer for interruption	I0 to I31 (32 points)	
	K	Decimal constant	K32768 to 32767 (16-bit instruction)	
			K2147483648 to 2147483647 (32-bit instruction)	
	H	Hexadecimal constant	H0 to FFFF (16 bit instruction)	
			H0 to FFFFFFFF (32-bit instruction)	

Table 3.3 Device List

POINT

The function of step relays (S) is identical to that of internal relays (M).

(1) Special relay list

The special relays are internal relays with special functions. They are mostly used as contacts to provide interlocks, timing pulse chains, etc. Table 3.4 shows the special relay list.
M9200 and following are used in conjunction with the MELSEC-NET data link system.

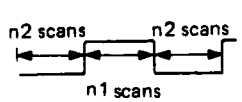
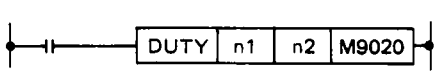
Number	Name	Description	Details
*1 M9000	Fuse blown	OFF: Normal ON: Fuse blown in an I/O module	• Turned on when one or more output unit fuses have blown. Remains on after normal status is restored.
*1 M9002	I/O unit verify error	OFF: Normal ON: Error	• Turned on when an I/O unit is removed from, or added to the system while the power is switched on. Remains on after normal status is restored.
*1 M9005	AC DOWN detection	OFF: AC supply normal ON: AC is down	• Turned on by a power failure of within 10ms. Reset when PC CPU is reset.
*1 M9006	Battery low	OFF: Normal ON: Battery low	• Turned on when battery voltage drops below that specified. Turned off when battery voltage is restored.
*1 M9007	Battery low latch	OFF: Normal ON: Battery low	• Turned on when battery voltage drops below that specified. Remains on after battery voltage is restored.
*1 M9008	Self-diagnostic error	OFF: No error ON: Error	• Turned on by self-diagnosed error.
M9009	Annunciator detection	OFF: No annunciator detected ON: Annunciator detected	• Turned on when OUT F or SET F instruction is executed. Switched off when all annunciators (F) are switched off.
*1 M9011	Operation error flag	OFF: No error ON: Error	• Turned on by an application instruction processing error. Remains on after normal status is restored.
M9012	Carry flag	OFF: Carry off ON: Carry on	• Carry flag used in application instructions.
M9016	Data memory clear flag	OFF: Ignore ON: Output clear	• Clears the data memory (other than special relays and special registers) in remote run mode from computer, etc. when M9016 is on.
M9017	Data memory clear flag	OFF: Ignore ON: Output clear	• Clears the unlatched data memory (other than special relays and special registers) in remote run mode from computer, etc. when M9017 is on.
M9020	User timing clock No. 0		• Scan dependent clock pulse. • After power on or CPU reset, the duty clock contacts are open. • On and off periods are specified in the DUTY instruction. 
M9021	User timing clock No. 1		
M9022	User timing clock No. 2		
M9023	User timing clock No. 3		
M9024	User timing clock No. 4		
M9030	0.1 second clock	0.05 seconds / 0.05 seconds	• Time dependent clock pulse: 0.1 second, 0.2 second, 1 second, 2 second, and 1 minute clocks. • Not scan dependent (i.e. will be switched during scan if corresponding time has elapsed). • Starts when power is turned on or CPU is reset.
M9031	0.2 second clock	0.1 seconds / 0.1 seconds	
M9032	1 second clock	0.5 seconds / 0.5 seconds	
M9033	2 second clock	1 seconds / 1 seconds	
M9034	1 minute clock	30 seconds / 30 seconds	

Table 3.4 Special Relay List

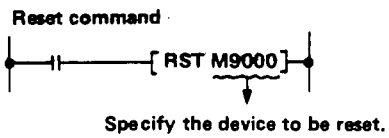
Number	Name	Description	Details
M9036	Normally ON	ON ——— OFF	• Used as dummy contacts for initialization and application instructions. • M9036 and M9037 are turned on and off independently of the key switch position on the CPU. M9038 and M9039 change depending on the key switch position. M9038 and M9039 are switched off if the key switch is in STOP position. M9038 is switched off (on for one scan only) and M9039 switch-on (off for one scan only) if the key switch is not in STOP position.
M9037	Normally OFF	ON OFF ———	
M9038	On only for 1 scan after run	ON OFF ⟷ 1 scan	
M9039	RUN flag (off only for 1 scan after run)	ON OFF ⟷ 1 scan	
M9040	PAUSE enable coil	OFF: PAUSE disabled ON: PAUSE enabled	• When RUN key switch is at PAUSE position or remote pause contact has turned on and if M9040 is on, the PC enters PAUSE mode and M9041 is turned on.
M9041	PAUSE status contact	OFF: During pause ON: Other than pause	
M9042	Stop status contact	OFF: During stop ON: Other than stop	
M9043	Sampling trace complete	OFF: During sampling trace ON: Sampling trace complete	• Tuned on to indicate that the sampling trace has been recorded the specified number of times. Reset when STRAR instruction is executed.
M9046	Sampling trace	OFF: Trace inactive ON: Trace active	• Switched on during sampling trace.
M9047	Sampling trace start	OFF: Sampling trace stop ON: Sampling trace start	• Sampling trace is started by switching on M9047 in the program. M9047 is automatically switched on if sampling is started from the GPP. By turning off M9047, sampling trace is stopped.
M9051	CHG instruction disable	ON: Disable OFF: Enable	
M9052	SEG instruction switching	OFF: Decode function to 7-segment display data ON: Partial refresh function	• The SEG instruction function is changed by switching M9052 on/off in the sequence program.
M9054	STEP RUN flag	OFF: Other than step run ON: During step run	• Switched on during step run.
M9055	Status latch complete flag	OFF: Not complete ON: Complete	• Turned on when status latch is completed. Turned off by reset instruction.
M9056	Main program P, I set request	ON: P, I set request OFF: Other than P, I set request	• Provides P, I set request after completion of program correction when correction of the other program (for example subprogram when main program is being run) is made during run. Turned off after setting is complete.
M9057	Subprogram P, I set request	ON: During P, I set request OFF: Except during P, I set request	
M9058	Main program P, I set complete	Pulsed on completion of P, I setting	• Pulsed on after completion of P, I setting.
M9059	Subprogram P, I set completion	Pulsed on completion of P, I setting	
*2 M9084	Error check	OFF: Checks enabled ON: Checks disabled	• Specify whether the following errors are to be checked or not after the END instruction is executed (to reduce END processing time): · Fuse blown · I/O unit verify error · Battery error

Table 3.4 Special Relay List (Continued)

POINT

(1) Special relays marked *1 above, are latched "on" and will remain on after normal status is restored. Switch then off as follows:

1) From the user program
Use the circuit shown on the right and turn on the reset command contact to clear the special relay M.



2) From the peripheral equipment (PU, GPP, PHP or HGP)
Use the test function to force reset the device. For the operation procedure, refer to the appropriate manual.

3) RESET the PC CPU using the key switch. This will reset the special relay.

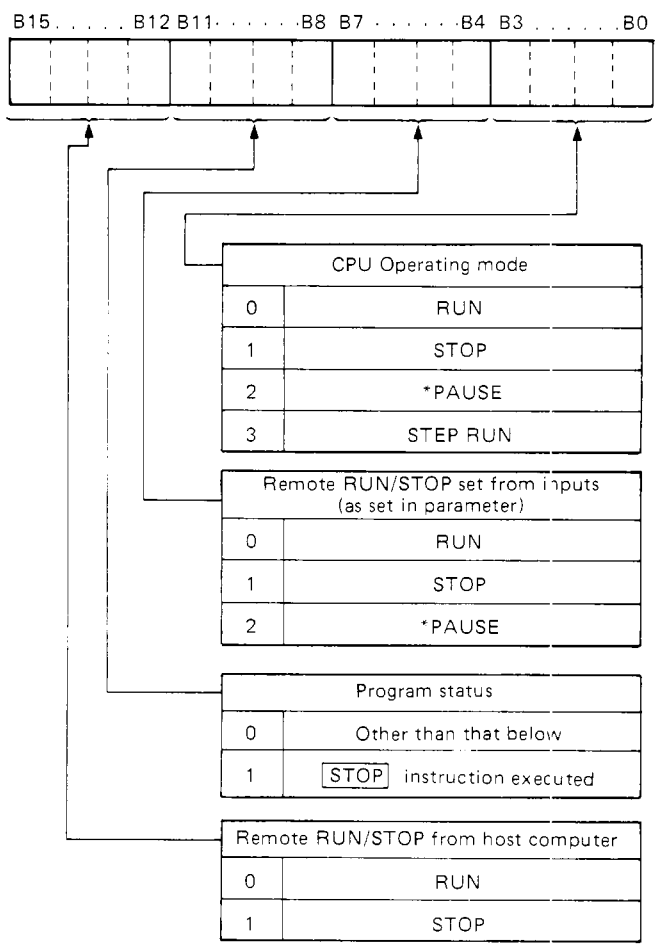
(2) M9084 marked *2 is switched on/off in the sequence program.

(2) Special register list

The special registers are data registers with special functions. Data should not be written to these registers (except those marked * in the table). Data may be read from the special registers and used as appropriate in the program. Table 3.5 shows the special register list.
D9200 and following are used in conjunction with the MELSEC-NET data link system.

Number	Name	Stored Data	Explanation
D9000	Fuse blown	Lowest unit number location with blown fuse	• Indicates the head I/O address of the lowest I/O unit number in which the fuse has blown. Use the hexadecimal monitor function on the peripheral equipment to read the data. (Cleared by resetting D9100 to D9107 to 0.)
D9002	I/O unit verify error	Lowest unit number location with I/O verify error	• Indicates the head I/O address of the lowest I/O unit number for which an I/O unit verify error has been detected (cause of error: addition or removal of an I/O unit while the power is on). Use the hexadecimal monitor function on the peripheral equipment to read the data. (Cleared by resetting D9116 to D9123 to 0.)
*D9005	AC DOWN counter	AC DOWN count	• 1 is added each time the input voltage drops to 80% or less of rated while the CPU unit is operating, and the value stored in BIN.
*D9008	Self-diagnostic error	Self-diagnostic error number	• Records the self-diagnosed error number.
D9009	Annunciator detection	Earliest annunciator number detected	• Records the number (in BIN) of the earliest annunciator coil (F) to be switched on by [OUT F□] or [SET F□]. • D9009 can be cleared by executing the [RST F□] or [LEDR] instruction or pressing INDICATOR RESET on CPU front. If another F number has been detected, the clearing of D9009 causes the next number to be stored in D9009.
D9011	Error step	Step number location of operation error	• Records the step number (in BIN) at which an application instruction processing error occured. Error data cannot be overwritten until special relay M9011 is reset by the user program.

Table 3.5 Special Register List

<table>
<tr><th>Number</th><th>Name</th><th>Stored Data</th><th>Explanation</th></tr>
<tr><td>D9015</td><td>CPU operating status</td><td>Operation status of CPU</td><td>
● The operating status of the CPU is stored in D9015 as shown below:

B15 . . . . . B12 B11 · · · · · B8 B7 · · · · · B4 B3 . . . . . B0
CPU Operating mode
0 RUN
1 STOP
2 *PAUSE
3 STEP RUN
Remote RUN/STOP set from inputs (as set in parameter)
0 RUN
1 STOP
2 *PAUSE
Program status
0 Other than that below
1 STOP instruction executed
Remote RUN/STOP from host computer
0 RUN
1 STOP

*: When M9040 (Pause enable) is off, and the CPU keyswitch is moved to PAUSE, the CPU remains in RUN mode.
</td></tr>
<tr><td>D9016</td><td>Program number</td><td>0: Main program (ROM)
1: Main program (RAM)
2: Subprogram (RAM)</td><td>● Indicates which sequence program is currently running. As a BIN number; 0, 1 or 2.</td></tr>
<tr><td>D9017</td><td>Scan time</td><td>Minimum scan time (in units of 10ms)</td><td>● Records the minimum program scan time as a BIN integer multiple of 10ms.</td></tr>
<tr><td>D9018</td><td>Scan time</td><td>Scan time (in units of 10ms)</td><td>● Records the previous program scan time as a BIN integer multiple of 10ms.</td></tr>
<tr><td>D9019</td><td>Scan time</td><td>Maximum scan time (in units of 10ms)</td><td>● Records the maximum program scan time as a BIN integer multiple of 10ms.</td></tr>
</table>

Table 3.5 Special Register List (Continued)

MNA 66132A

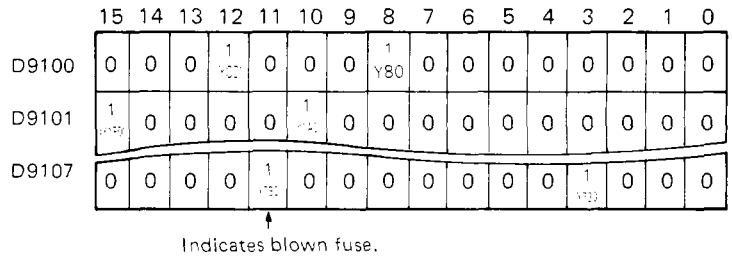
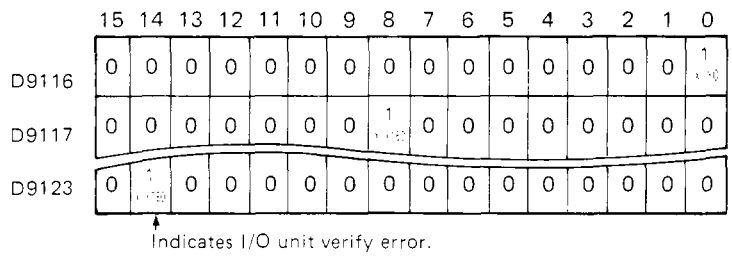
Number	Name	Stored Data	Explanation
*D9020	Constant scan	Constant scan time (Set by user in 10ms increments)	Sets the interval between consecutive program starts in multiples of 10ms. 0: No setting 1 to 19: Set. Program is executed at intervals of (set value) x 10ms. (See Section 3.2.10.)
D9044	For sampling trace	Step or time for sampling trace	• Determines the sampling trace operating conditions as a BIN number. For scan ——— 0 For time ——— Time (in units of 10ms)
*D9100 *D9101 *D9102 *D9103 *D9104 *D9105 *D9106 *D9107	Fuse blown unit	Bit map of I/O units with blown fuses	• Indicates the output unit numbers with blown fuses. Indication is in blocks of 16 I/O points and parameter I/O assignment is valid.  (Data is latched and must be cleared from the user program)
*D9116 *D9117 *D9118 *D9119 *D9120 *D9121 *D9122 *D9123	I/O unit verify error	Bit map of I/O units with verify errors	• Indicates the I/O unit numbers with I/O unit verify errors. (Cause of error: addition or removal of an I/O unit while the power is on) Parameter I/O assignment is valid.  (Data is latched and must be cleared from the user program.)
D9124	Number of detected annunciator signals	Number of unprocessed signals	• 1 is add to the contents of D9124 each time any of the annunciator (F) coils is switched on (by OUT F□ or SET F□). 1 is subtracted from the contents of D9124 each time an F coil is reset (by RST F□ , LEDR or INDICATOR RESET). • The number is shored in BIN and is ≤ 8.

Table 3.5 Special Register List (Continued)

Number	Name	Stored Data	Explanation
D9125 D9126 D9127 D9128 D9129 D9130 D9131 D9132	Detected annunciator numbers	Records and queues detected annunciator numbers	• Registers D9125 to D9132 record the annunciator (F) numbers in BIN in the order in which they occur on a First in First out basis. • Annunciator numbers are removed from any place in the queue by applying the [RST F□] instruction. Subsequent entries then move up one place. • The annunciator number at the head of the queue is cleared by the [LEDR] instruction or INDICATIOR RESET and subsequent entries move up by one place. • The 9th annunciator number is ignored until there is room in the queue.

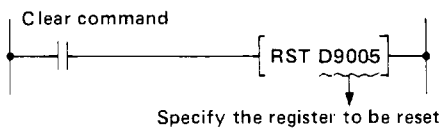
	[SET F50]	[SET F25]	[SET F99]	[RST F25]	[SET F15]	[SET F70]	[SET F65]	[SET F38]	[SET F□□]	[SET F15]	[SET F□□]	[LEDR] INDICATOR RESET	
D9009	0	50	50	50	50	50	50	50	50	50	50	50	99	15
D9124	0	1	2	3	2	3	4	5	6	7	8	8	8	7
D9125	0	50	50	50	50	50	50	50	50	50	50	50	99	15
D9126	0	0	25	25	99	99	99	99	99	99	99	99	15	70
D9127	0	0	0	99	0	15	15	15	15	15	15	15	70	65
D9128	0	0	0	0	0	0	70	70	70	70	70	70	65	38
D9129	0	0	0	0	0	0	0	65	65	65	65	65	38	110
D9130	0	0	0	0	0	0	0	0	38	38	38	38	110	151
D9131	0	0	0	0	0	0	0	0	0	110	110	110	151	210
D9132	0	0	0	0	0	0	0	0	0	0	151	151	210	

Table 3.5 Special Register List (Continued)

POINT

(1) Special registers marked * above, are latched and their data will remain unchanged after normal status is restored. Clear the registers as follows:

1) From the user program
Use the circuit shown on the right and turn on the clear command contact to clear the register contents.



2) From the peripheral equipment (PU, GPP, PHP or HGP)
Use the test function to change the present value of the register to 0. For the operation procedure, refer to the appropriate manual.

3) By moving the RESET key switch at the CPU front to the RESET position, the special register is set to "0".

3.2.4 Instruction list

Instructions available for the A3HCPU programmable controller may be classified into sequence instructions, basic instructions, and application instructions as shown in Table 3.6.

Classification of instructions		Description
Sequence instructions		Instructions for relay control circuit
Basic instructions	Comparison instructions	Comparisons such as =, >, and <
	Arithmetic instructions	Addition, subtraction, multiplication, and division of BIN and BCD
	BCD ↔ BIN conversion instructions	Conversions from BCD to BIN and BIN to BCD
	Data transfer instructions	Transfer of specified data
	Program branch instructions	Sequence program conditional and unconditional branch instructions
Application instruction	Display instructions	Display onto indicator on front of CPU unit
	Logical operation instructions	Logical operations such as logical sum and logical product
	Rotation instructions	Rotation of specified data
	Shift instructions	Shift of specified data
	Data processing instructions	Data processing such as 16-bit data search, decode, and encode
	FIFO instructions	Read/write of FIFO table
	ASCII conversion instruction	Conversion of ASCII characters into ASCII code
	Special unit instructions	Data transfer to and from special unit
	Others	Instructions which are not included in the above classification, such as WDT reset, and carry flag set/reset.

Table 3.6 Classification of instructions

A list of all the instructions is given in the following pages in the order given above.

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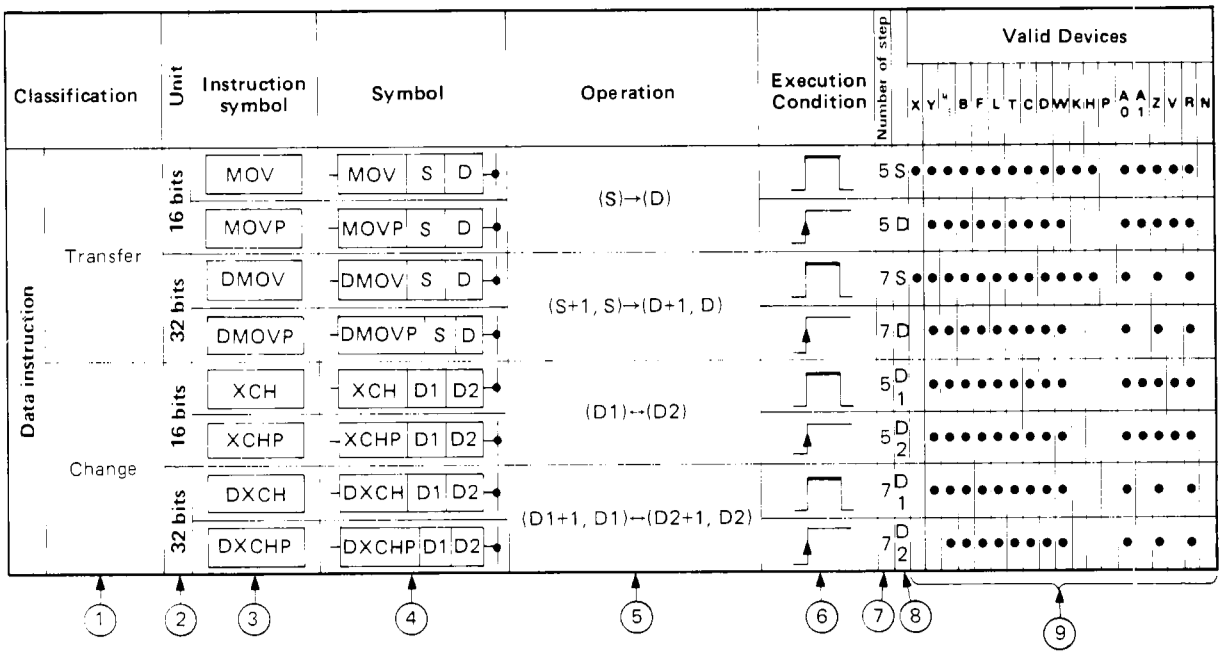
(1) How to use the instruction list.

The instructions listed in Section (2) to (4) are given in the following format.



① . . . . Classifies the instruction by application.
② . . . . Indicates whether the instruction processes bit, word or double-word data.

Unit of Processing	Device	Number of devices required
16 bits	X, Y, M, L, F, B	Max. 16 points in units of 4 points.
	T, C, D, W, R, A0, A1, Z, V	1 point
32 bits	X, Y, M, L, F, B	Max. 32 points in units of 4 points.
	T, C, D, W, R, A0, Z	2 points

③ . . . . Indicates the instruction symbol used during programming.
The instruction set which operates on numerical data, is based on 16 bit data processing instructions. These may be modified as follows:

Add a D infront of (or, in some cases, after) the instruction symbol to define if as a 32 bit processing instruction.

Example: + ⟹ D+

16-bit instruction — 32-bit instruction

Add a P after the instruction to define it as being operated only by a leading edge in the preceding contact continuity.

Example: + ⟹ +P

Instruction executed continuously by preceding contact continuity

Instruction executed only at the leading edge of preceding contact continuity.

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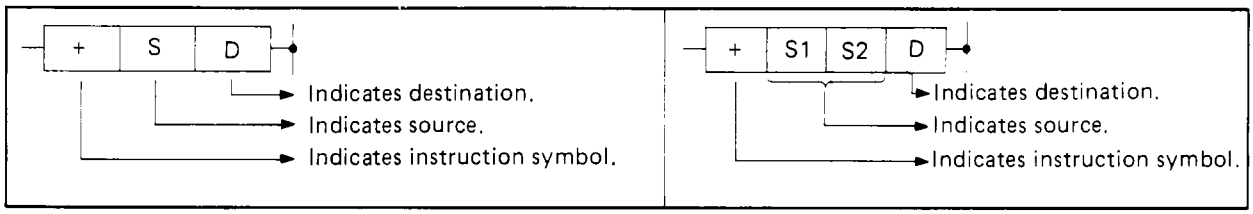
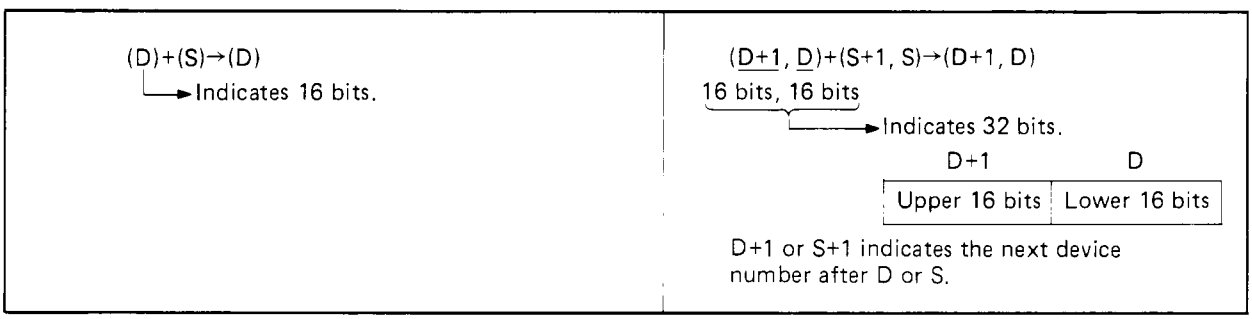
④ . . . .Indicates the symbol used in the ladder diagram and the significance of the data in the instruction.



Destination: Indicates the destination of the operation result.
Source: Indicates the source of the data for the operation.

⑤ . . . .Indicates the operation.



⑥ . . . .Indicates the condition of execution for each instruction as described below:

Symbol	Execution Condition
No entry	Instruction is always executed. (i.e. no preceding contact logic)
	The instruction is executed continuously all the time that the contacts preceding it allow continuity. As soon as continuity ends, execution of the instruction stops and it is not processed.
	The instruction is executed once when continuity from the preceding contacts provides a leading edge to the instruction "coil". Once the leading edge is provided, the instruction is executed once only, even if the preceding contact continuity is maintained, until continuity is broken and then re-established.
	The instruction is executed once only when continuity from the preceding contacts provides a trailing edge to the instruction "coil". Once the trailing edge is provided, the instruction is executed once only, even if the preceding contact continuity remains broken, until continuity is re-established and then broken.

⑦ . . . .Indicates the number of program steps required for each instruction. The number of steps changes depending on conditions for full details, refer to the instruction in the programming manual.

⑧ . . . .Indicates which devices may be used as source(s) and/or destination (D) devices.

⑨ . . . .A ● in a device column, next to S and/or D indicates that the device is valid in that instruction.

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(2) Sequence instructions

22 sequence instructions: —

Classification	Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps		Valid Devices (X Y B F L T C D W K H P A0 A1 Z V R N)
Sequence instruction		LD		The first, N/O, contact in a ladder rung (or block)		1		● ● ● ● ● ● ● ●
		LDI		The first, N/C contact in a ladder rung (or block)		1		● ● ● ● ● ● ● ●
		AND		Logical product (N/O series contact)		1		● ● ● ● ● ● ● ●
		ANI		Logical product NOT (N/C series contact)		1		● ● ● ● ● ● ● ●
		OR		Logical sum (N/O parallel contact)		1		● ● ● ● ● ● ● ●
		ORI		Logical sum NOT (N/C parallel contact)		1		● ● ● ● ● ● ● ●
		ANB		AND between logical blocks (series connection between blocks)		1		
		ORB		OR between logical blocks (Parallel connection between blocks)		1		
		OUT		Device coil (OUT T/C must include D or K data)		1 3		● ● ● ● ● ● ● ● ● ●
		SET	SET D	Set device		1/3 3	D D	● ● ● ●
		RST	RST D	Reset device		1/3 3	D D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		MC	MC n D	Master control start		5	n D	● ● ● ● ● ●
		MCR	MCR n	Master control reset		3	n	●
		PLS	PLS D	Produces a pulse lasting one program scan time from the specified device.		3	D	● ● ● ● ●
		PLF	PLF D	Produces a pulse lasting one program scan time from the specified device		3	D	● ● ● ● ●
		SFT	SFT D	1-bit device shift		3	D	● ● ● ● ●
		SFTP	SFTP D			3	D	● ● ● ● ●
		NOP	—	No operation		1		
		END	—	Return to step 0 Must be wirtten at the end of program.		1		
		MPS	MPS MRD MPP	Store result of preceding operations		1		
		MRD		Read result of preceding operations		1		
		MPP		Read and reset result of preceding operations		1		

(3) Basic instructions

133 basic instructions:

Classification	Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps	Valid Devices
Comparison instruction	16 bits	LD =	S1 S2	Continuity when (S1) = (S2) Non-continuity when (S1) ≠ (S2)		5 / 7	S1 ● ● ●

Classification	Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps	Valid Devices (X Y M S B F L T C D W K H P A0 A1 Z V R N)
Comparison instruction	16 bits	LD< =	S1 S2	Continuity when (S1) ≤ (S2) Non-continuity when (S1) > (S2)		5 / 7	S1 ●
		AND< =	S1 S2			5 / 7	
		OR< =	S1 S2			5 / 7	S2 ●
	32 bits	LDD< =	D S1 S2	Continuity when (S1+1, S1) ≤ (S2+1, S2) Non-continuity when (S1+1, S1) > (S2+1, S2)		11	S1 ●
		ANDD< =	D S1 S2			11	
		ORD< =	D S1 S2			11	S2 ●
	16 bits	LD<	S1 S2	Continuity when (S1) < (S2) Non-continuity when (S1) ≥ (S2)		5 / 7	S1 ●
		AND<	S1 S2			5 / 7	
		OR<	S1 S2			5 / 7	S2 ●
	32 bits	LDD<	D S1 S2	Continuity when (S1+1, S1) < (S2+1, S2) Non-continuity when (S1+1, S1) ≥ (S2+1, S2)		11	S1 ●
		ANDD<	D S1 S2			11	
		ORD<	D S1 S2			11	S2 ●
BIN arithmetic operation instruction	16 bits	LD =	S1 S2	Continuity when (S1) = (S2) Non-continuity when (S1) ≠ (S2)		5 / 7	S1 ●
		AND =	S1 S2			5 / 7	
		OR =	S1 S2			5 / 7	S2 ●
	32 bits	LDD =	D S1 S2	Continuity when (S1+1, S1) = (S2+1, S2) Non-continuity when (S1+1, S1) ≠ (S2+1, S2)		11	S1 ●
		ANDD =	D S1 S2			11	
		ORD =	D S1 S2			11	S2 ●

Classification	Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps		Valid Devices
BIN arithmetic operation instruction								X Y M S B F L T C D W K H P A0 A1 Z V R N
+	16 bits	+	+ S D	(D) + (S) → (D)		5	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		+P	+P S D			5	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	32 bits	D+	D+ S D	(D+1, D) + (S+1, S) → (D+1, D)		9	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		D + P	D + P S D			9	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	16 bits	+	+ S1 S2 D	(S1) + (S2) → (D)		7	S1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
							S2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		+P	+P S1 S2 D			7	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	32 bits	D+	D+ S1 S2 D	(S1+1, S1) + (S2+1, S2) → (D+1, D)		11	S1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
							S2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		D + P	D + P S1 S2 D			11	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
−	16 bits	−	− S D	(D) − (S) → (D)		5	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		−P	−P S D			5	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	32 bits	D−	D− S D	(D+1, D) − (S+1, S) → (D+1, D)		9	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		D − P	D − P S D			9	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	16 bits	−	− S1 S2 D	(S1) − (S2) → (D)		7	S1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
							S2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		−P	−P S1 S2 D			7	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	32 bits	D−	D− S1 S2 D	(D+1, D) − (S−1, S) → (D+1, D)		11	S1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
							S2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		D − P	D − P S1 S2 D			11	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
*	16 bits	*	* S1 S2 D	(S1) × (S2) → (D+1, D)		7	S1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
							S2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		*P	*P S1 S2 D			7	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	32 bits	D*	D* S1 S2 D	(S1+1, S1) × (S2−1, S2) · (D+3, D+2, D−1, D)		11	S1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
							S2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		D*P	D*P S1 S2 D			11	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●

Classification	Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps		Valid Devices
BIN arithmetic operation instruction	16 bits	/	/ S1 S2 D	(S1) ÷ (S2) → Quotient (D), Remainder (D+1)		7	S1	● ●
		/P	/P S1 S2 D			7	S2	● ●
							D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	32 bits	D/	D/ S1 S2 D	(S1+1, S1) ÷ (S2+1, S2) → Quotient (D+1, D), Remainder (D+3, D+2)		9	S1	● ●
		D/P	D/P S1 S2 D			9	S2	● ●
							D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
+1	16 bits	INC	INC D	(D) + 1 → (D)		3	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		INCP	INCP D			3		
	32 bits	DINC	DINC D	(D+1, D) + 1 → (D+1, D)		3	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		DINCP	DNCP D			3		
BCD arithmetic operation instruction	16 bits	DEC	DEC D	(D) − 1 → (D)		3	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		DECP	DECP D			3		
−1	32 bits	DDEC	DDEC D	(D+1, D) − 1 → (D−1, D)		3	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		DDECP	DDECP D			3		
	BCD 4 digits	B+	B+ S D	(D) + (S) → (D)		7	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		B+P	B+P S D			7	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	BCD 8 digits	DB+	DB+ S D	(D−1, D) + (S+1, S) → (D+1, D)		9	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		DB+P	DB+P S D			9	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	BCD 4 digits	B+	B+ S1 S2 D	(S1) + (S2) → (D)		9	S1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		B+P	B+P S1 S2 D			9	S2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
							D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	BCD 8 digits	DB+	DB+ S1 S2 D	(S1+1, S1) + (S2+1, S2) → (D+1, D)		11	S1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		DB+P	DB+P S1 S2 D			11	S2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
							D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●

Classification	Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps	Valid Devices
BCD arithmetic operation instruction	BCD 4 digits	B–	B– S D	(D) – (S) → (D)		7	S
		B – P	B – P S D			7	D
	BCD 8 digits	DB–	DB– S D	(D+1, D) – (S+1, S) → (D+1, D)		9	S
		DB – P	DB – P S D			9	D
	BCD 4 digits	B–	B– S1 S2 D	(S1) – (S2) → (D)		9	S1
							S2
		B – P	B – P S1 S2 D			9	D
	BCD 8 digits	DB	DB– S1 S2 D	(S1+1, S1) – (S2+1, S2) → (D+1, D)		11	S1
							S2
		DB – P	DB–P S1 S2 D			11	D
	BCD 4 digits	B*	B* S1 S2 D	(S1) × (S2) → (D+1, D)		9	S1
							S2
		B*P	B*P S1 S2 D			9	D
	BCD 8 digits	DB*	DB* S1 S2 D	(S1+1, S1) × (S2+1, S2) → (D+3, D+2, D+1, D)		11	S1
							S2
		DB*P	DB*P S1 S2 D			11	D
	BCD 4 digits	B/	B/ S1 S2 D	(S1) ÷ (S2) → Quotient (D) Remainder (D+1)		9	S1
							S2
		B/P	B/P S1 S2 D			9	D
	BCD 8 digits	DB/	DB/ S1 S2 D	(S1+1, S1) ÷ (S2+1, S2) → Quotient (D+1, D), Remainder (D+3, D+2)		11	S1
							S2
		DB/P	DB/P S1 S2 D			11	D
BIN BCD conversion instruction	BCD 16 bits	BCD	BCD S D	BCD conversion (S) → (D) BIN (0 ~ 9999)		5	S
		BCDP	BCDP S D			5	D
	BCD 32 bits	DBCD	DBCD S D	BCD conversion (S1+1, S1) → (D+1, D) BIN (0 ~ 99999999)		9	S
		DBCDP	DBCDP S D			9	D

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Classification		Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps		Valid Devices (X Y M B F L T C D W K H P A0 A1 Z V R N)
BCD → BIN conversion instruction	BIN	16 bits	BIN	BIN S D	BIN conversion (S) → (D); BCD (0 ~ 9999)		5	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			BINP	BINP S D		↑	5	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		32 bits	DBIN	DBIN S D	BIN conversion (S1+1, S1) → (D+1, D); BCD (0 ~ 99999999)		9	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			DBINP	DBINP S D		↑	9	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
Data transfer instruction	Transfer	16 bits	MOV	MOV S D	(S) → (D)		5	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			MOVP	MOVP S D		↑	5	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		32 bits	DMOV	DMOV S D	(S+1, S) → (D+1, D)		7	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			DMOVP	DMOVP S D		↑	7	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	Change	16 bits	XCH	XCH D1 D2	(D1) → (D2)		5	D1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			XCHP	XCHP D1 D2		↑	5	D2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		32 bits	DXCH	DXCH D1 D2	(D1+1, D1) ↔ (D2+1, D2)		7	D1	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			DXCHP	DXCHP D1 D2		↑	7	D2	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	Undefined transfer	16 bits	CML	CML S D	$\overline{(S)}$ → (D)		5	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			CMLP	CMLP S D		↑	5	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
		32 bits	DCML	DCML S D	$\overline{(S+1, S)}$ → (D+1, D)		7	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			DCMLP	DCMLP S D		↑	7	D	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	Block transfer	16 bits	BMOV	BMOV S D n	(S) → (D), n		9	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			BMOVP	BMOVF S D n		↑	9	D, n	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
	Repeat data block transfer	16 bits	FMOV	FMOV S D n	(S) → (D), n		9	S	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
			FMOVP	FMOVP S D n		↑	9	D, n	● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●

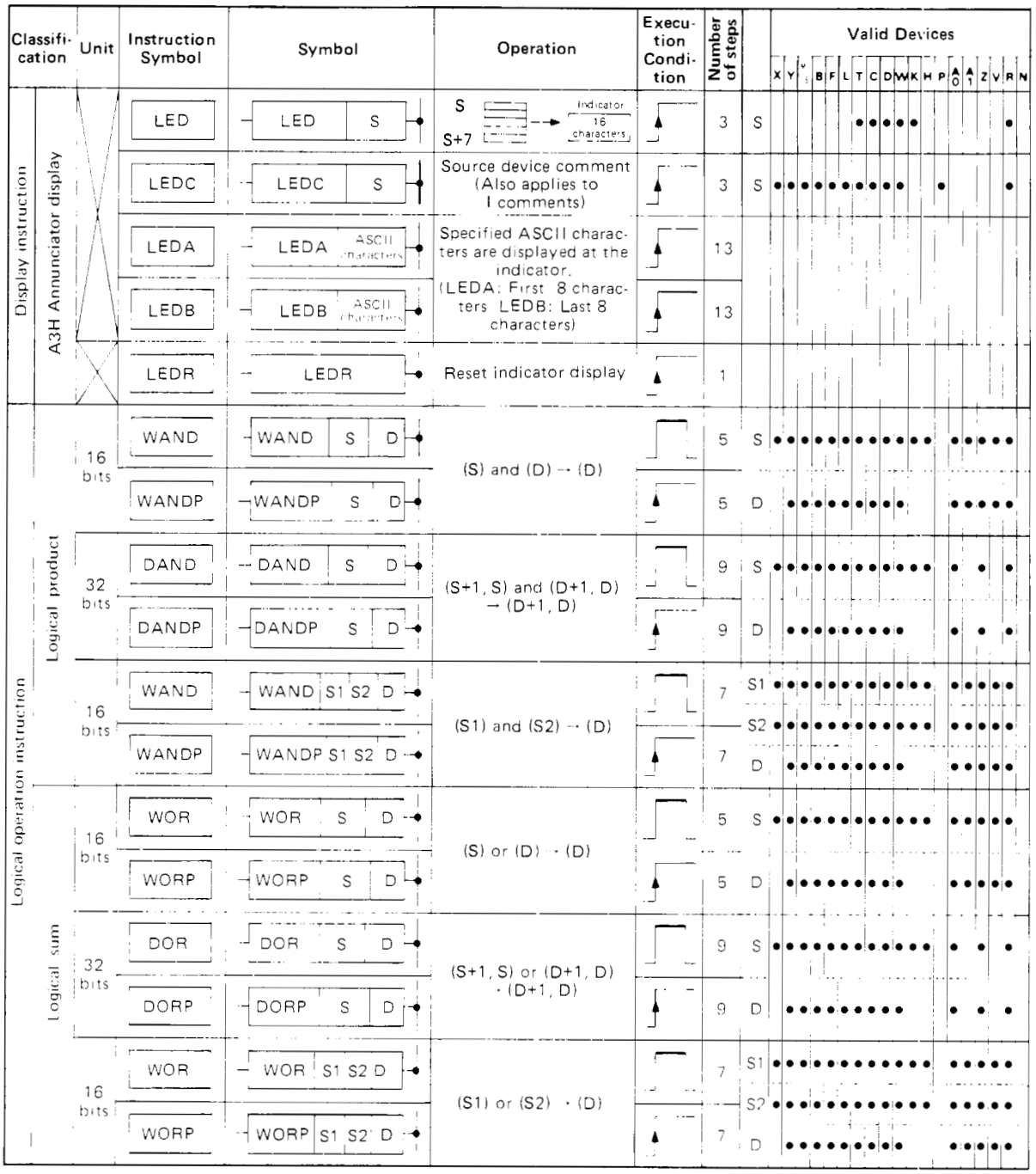
Classification	Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps	Valid Devices (X Y M B F L T C D W K H P A0 A1 Z V R N)
Jump		CJ	CJ P**	Jump to P** after input condition holds.		3	P
		SCJ	SCJ P**	Jump to P** at the next scan after input condition holds.	See programming manual	3	P
		JMP	JMP P**	Jump to P** unconditionally.		3	P
Program call		FEND	FEND	Sequence program processing complete.		1	
Subroutine call		CALL	CALL P**	Subroutine program P** is executed after input condition holds.		3	P
		CALLP	CALLP P**			3	P
Return		RET	RET	Return from subroutine program to sequence program.		1	
		IRET	IRET	Return from interrupt program to sequence program.		1	
Disable		DI	DI	Disable interrupt program (Inputs and outputs both in direct mode) / Disable interrupt program and disable link refresh (Inputs and or outputs in refresh mode)		1	
Enable		EI	EI	Enable interrupt program (Inputs and outputs both in direct mode) / Enable interrupt program and enable link refresh (Inputs and or outputs in refresh mode)		1	
Repeat		FOR	FOR n	Program between FOR and NEXT is repeated "n" times.		3	n
		NEXT	NEXT			1	
Stop		STOP	STOP	After input condition holds, outputs are reset and sequence program is stopped. When RUN key switch is set to RUN position again sequence program is resumed		1	
Change		CHG	CHG	Switch from main to sub program and vica versa.		1	
Micro-computer program call		SUB	SUB n	Call micro computer subroutine		3	n
		SUBP	SUBP n			3	n
		COM	COM	Link refresh. Intiates general data processing.		1	

POINT

(1) General data processing by the COM instruction involves the following:
- Batch write (buffer memory, sequence programs, parameters)
- Batch read (buffer memory, sequence programs, parameters)
- Monitoring
- Test (set, reset)
- Remote run/stop/pause

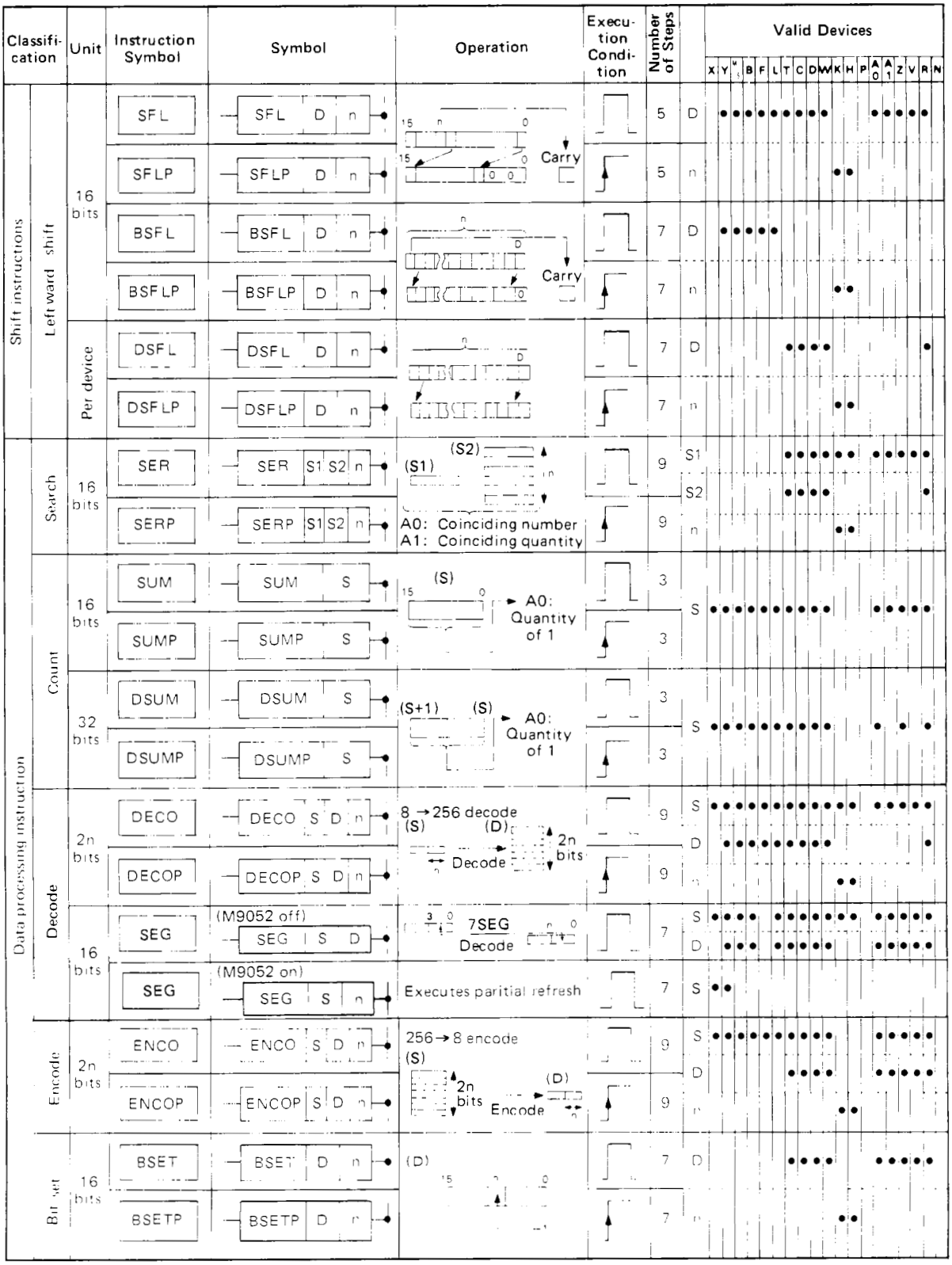
(4) Application instructions

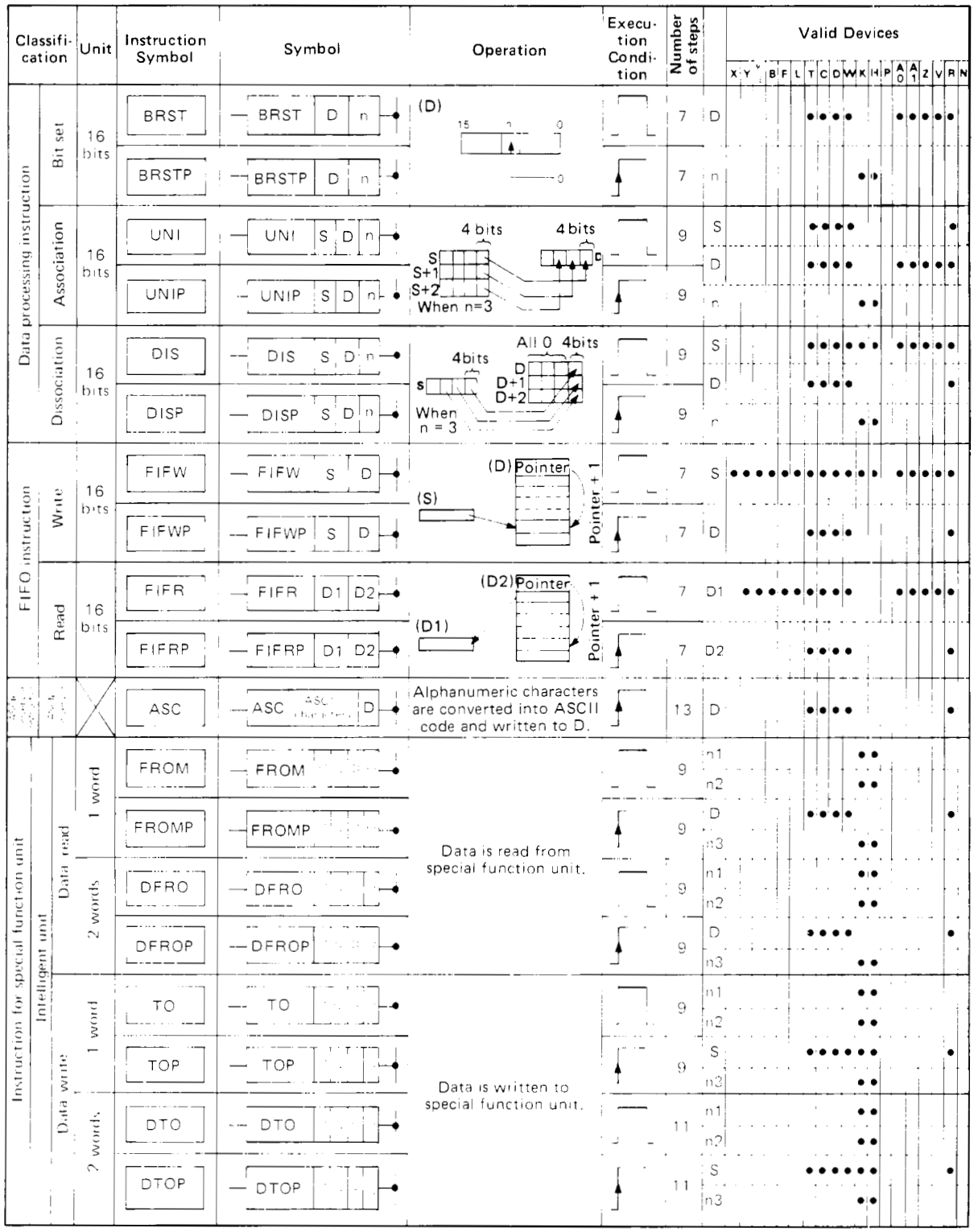
108 Application instructions:



Classification		Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps		Valid Devices
Logical operation instruction	Exclusive logical sum	16 bits	WXOR	WXOR S D	(S) Xor (D) → (D)		5	S	X Y M B F L T C D W K H P A0 A1 Z V R N
			WXORP	WXORP S D			5	D	
		32 bits	DXOR	DXOR S D	(S+1, S) Xor (D+1, D) → (D+1, D)		9	S	
			DXORP	DXORP S D			9	D	
		16 bits	WXOR	WXOR S1 S2 D	(S1) Xor (S2) → (D)		7	S1	
								S2	
			WXORP	WXORP S1 S2 D			7	D	
	NOT exclusive logical sum	16 bits	WXNR	WXNR S D	(S) Xor (D) → (D)		5	S	
			WXNRP	WXNRP S D			5	D	
		32 bits	DXNR	DXNR S D	(S+1, S) Xor (D+1, D) → (D+1, D)		9	S	
			DXNRP	DXNRP S D			9	D	
		16 bits	WXNR	WXNR S1 S2 D	(S1) Xor (S2) → (D)		7	S1	
								S2	
			WXNRP	WXNRP S1 S2 D			7	D	
	2's complement	16 bits	NEG	NEG D	$\overline{(D)} + 1 \rightarrow (D)$		3	D	
			NEGP	NEGP D			3		
Rotation instruction	Right ward rotation	16 bits	ROR	ROR n	Carry b15 A0 b0 "n" bit rotate to right		3	n	
			RORP	RORP n			3		
			RCR	RCR n	A0 b15 b16-n b0 Carry "n" bit rotate to right		3	n	
			RCRP	RCRP n			3		

Classification		Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of Steps	Valid Devices
Rotation instruction	Right ward rotation	32 bits	DROR	DROR n	Carry, "n" bit rotate to right		3	n
			DRORP	DRORP n			3	
			DRCR	DRCR n	Carry, "n" bit rotate to right		3	n
			DRCRP	DRCRP n			3	
	Left ward rotation	16 bits	ROL	ROL n	Carry, "n" bit rotate to left		3	n
			ROLP	ROLP n			3	
			RCL	RCL n	Carry, "n" bit rotate to left		3	n
			RCLP	RCLP n			3	
		32 bits	DROL	DROL n	Carry, "n" bit rotate to left		3	n
			DROLP	DROLP n			3	
			DRCL	DRCL n	Carry, "n" bit rotate to left		3	n
			DRCLP	DRCLP n			3	
Shift instruction	Right ward shift	16 bits	SFR	SFR D n	Carry		5	D
			SFRP	SFRP D n			5	n
			BSFR	BSFR D n	Carry		7	D
			BSFRP	BSFRP D n			7	n
		Per device	DSFR	DSFR D n			7	D
			DSFRP	DSFRP D n			7	n


Classification
Unit
Instruction Symbol
Symbol
Operation
Execution Condition
Number of Steps
Valid Devices
Shift instructions
Leftward shift
Per device
16 bits
SFL
SFLP
BSFL
BSFLP
DSFL
DSFLP
Carry
Data processing instruction
Search
SER
SERP
(S1)
(S2)
A0: Coinciding number
A1: Coinciding quantity
Count
SUM
SUMP
DSUM
DSUMP
(S)
(S+1)
A0: Quantity of 1
32 bits
Decode
2n bits
DECO
DECOP
8 → 256 decode
Decode
SEG
(M9052 off)
(M9052 on)
7SEG
Executes paritial refresh
Encode
ENCO
ENCOP
256 → 8 encode
Bit set
BSET
BSETP


Classification
Unit
Instruction Symbol
Symbol
Operation
Execution Condition
Number of steps
Valid Devices
X Y M B F L T C D W K H P A0 A1 Z V R N
Data processing instruction
Bit set
16 bits
BRST
BRSTP
(D)
15 n 0
7
D
n
Association
UNI
UNIP
4 bits
S
S+1
S+2
When n=3
9
S
D
Dissociation
DIS
DISP
All 0 4bits
D
D+1
D+2
When n = 3
FIFO instruction
Write
FIFW
FIFWP
(D) Pointer
(S)
Pointer + 1
Read
FIFR
FIFRP
(D2) Pointer
(D1)
ASC
Alphanumeric characters are converted into ASCII code and written to D.
13
Instruction for special function unit
Intelligent unit
Data read
1 word
2 words
FROM
FROMP
DFRO
DFROP
Data is read from special function unit.
n1
n2
n3
Data write
TO
TOP
DTO
DTOP
Data is written to special function unit.

Classification		Unit	Instruction Symbol	Symbol	Operation	Execution Condition	Number of steps		Valid Devices
Other instructions	Data link unit (Data read)	1 word	LRDP	LRDP n1 S D n2	Data is read from local station.		11	n1 S	X Y M B F L T C D W K H P A0 A1 Z V R N
	Data link unit (Data write)		LWTP	LWTP n1 D S n2	Data is written to local station.		11	D n2	
	Data link unit (Data read)		RFRP	RFRP n1 n2 D n3	Data is read from special function unit in remote station.		11	n1 n2	
	Data link unit (Data write)		RTOP	RTOP n1 n2 D n3	Data is written to special function unit in remote station.		11	D n3	
	W/DT reset		WDT	WDT	WDT is reset in sequence program.		1		
			WDTP	WDTP					
	Status latch Set		SLT	SLT	Data specified in parameters is written to PC memory status latch area		1		
	Status latch Reset		SLTR	SLTR	Resets the status latch and re-enables the SLT instruction.		1		
	Sampling trace Set		STRA	STRA	Data specified in parameters is written to PC memory sampling trace area		1		
	Sampling trace Reset		STRAR	STRAR	Resets the sampling trace and re-enables the STRA instruction.		1		
	Carry Set	1 bit	STC	STC	Carry flag contact (M9012) is turned on.		1		
	Carry Reset		CLC	CLC	Carry flag contact (M9012) is turned off.		1		
	Timing clock	1 bit	DUTY	DUTY n1 n2 D	Sets up duty clock shown below Special register D: n1 scan, n2 scan M9020 to M9024 only, are valid for D.		7	n1 n2 D	
	ASCII print		PR	PR S D	Transfer of any number of ASCII codes to specified outputs.		7	S D	
			PRC	PRC S D	Transfer of ASCII comment data to specified outputs		7	S D	

POINT

The shaded CHG, PR and SEG instructions differ in specifications from those of the A1(E), A2(E), A3(E)CPUs. For further details, see Appendix 1.

3.2.5 Timer processing and accuracy

With continuity in front of a timer coil, the timer present value and contact status are updated after the execution of the END (or FEND) instruction and the timer contacts close after the timer has timed out. When the continuity is removed from in front of the timer coil, the present value is reset to 0 (retentive timers retain their present value and are reset using the RST command), and the timer contacts open.
If a timer is jumped, as in the example below, after it has started timing, it continues to time even if the preceding continuity is removed. (This is because the PC is no longer scanning the jumped program area.)

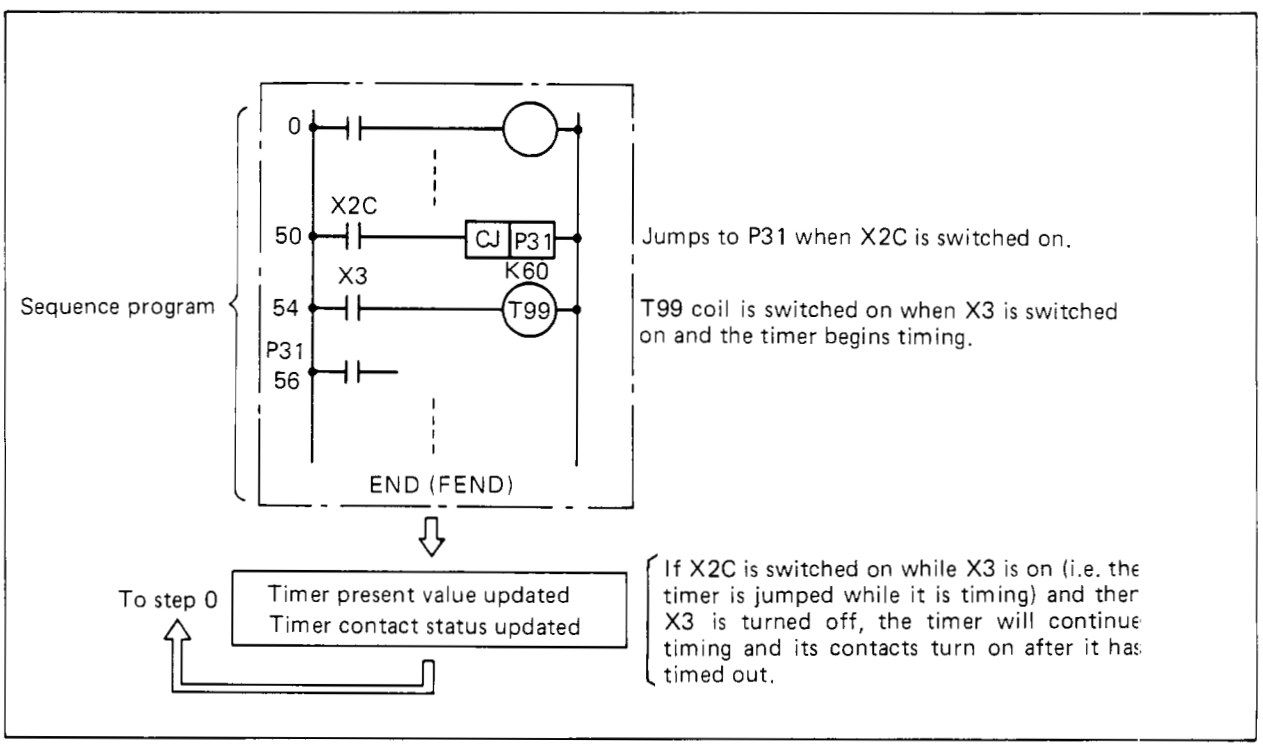
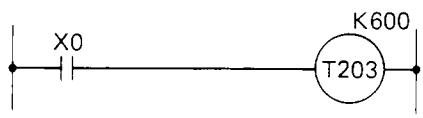

Sequence program
0
X2C
50
CJ P31
K60
X3
54
T99
P31
56
END (FEND)
Jumps to P31 when X2C is switched on.
T99 coil is switched on when X3 is switched on and the timer begins timing.
To step 0
Timer present value updated
Timer contact status updated
If X2C is switched on while X3 is on (i.e. the timer is jumped while it is timing) and then X3 is turned off, the timer will continue timing and its contacts turn on after it has timed out.

Fig. 3.1 Timer Processing

The timer present value update timing and accuracy in direct and refresh modes are explained on the following pages.
When the input (X) is used as a condition contact in front of the timer coil, accuracy differs between modes. For any other device used as a condition contact, see direct mode processing.

(1) Present value update timing and accuracy in direct mode

Ladder example



T203 contact is switched on 6 seconds after X0 is switched on. (T203 is a 10ms timer.)

Timer timing

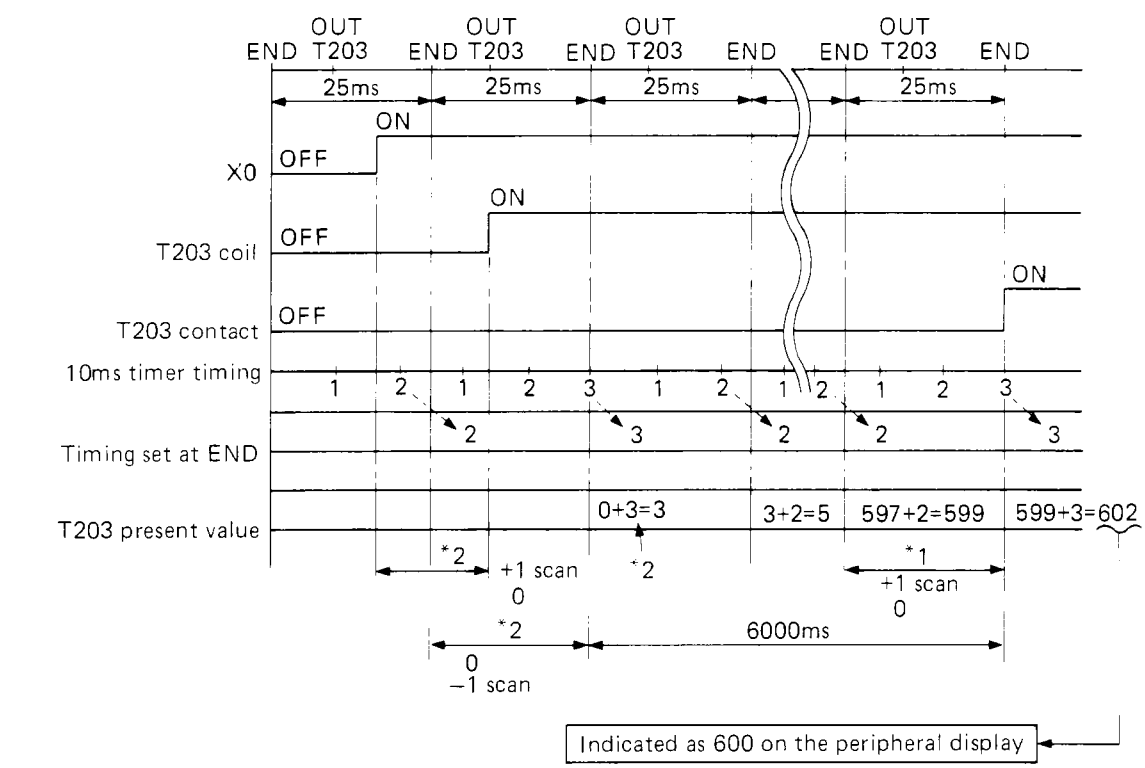


Fig. 3.2 Timer Timing

T203 time-out period includes the following errors:

*1: 10ms timer error (+1 scan time)
*2: Error depending on timing of timer input continuity and location of the OUT T□ instruction in program (±1 scan time)

A 10ms timer's accuracy is therefore $\begin{matrix}+2 \text{ scan time} \\ -1 \text{ scan time}\end{matrix}$ $\left(\begin{matrix}+0.05 \\ -0.025\end{matrix}\right.$ seconds in Fig. 3.2).

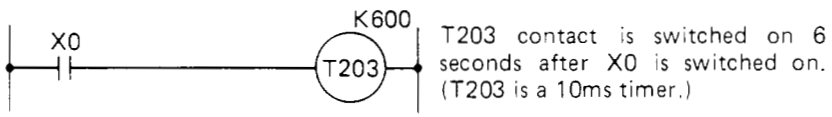
POINT

(1) The same applies to the accuracy of a 100ms timer, i.e $\begin{matrix}+2 \text{ scan time} \\ -1 \text{ scan time}\end{matrix}$

(2) Contact status is updated only after the END instruction is processed, regardless of the timer coil status during any scan.

(2) Update timing and accuracy in refresh mode

Ladder example



Timer timing

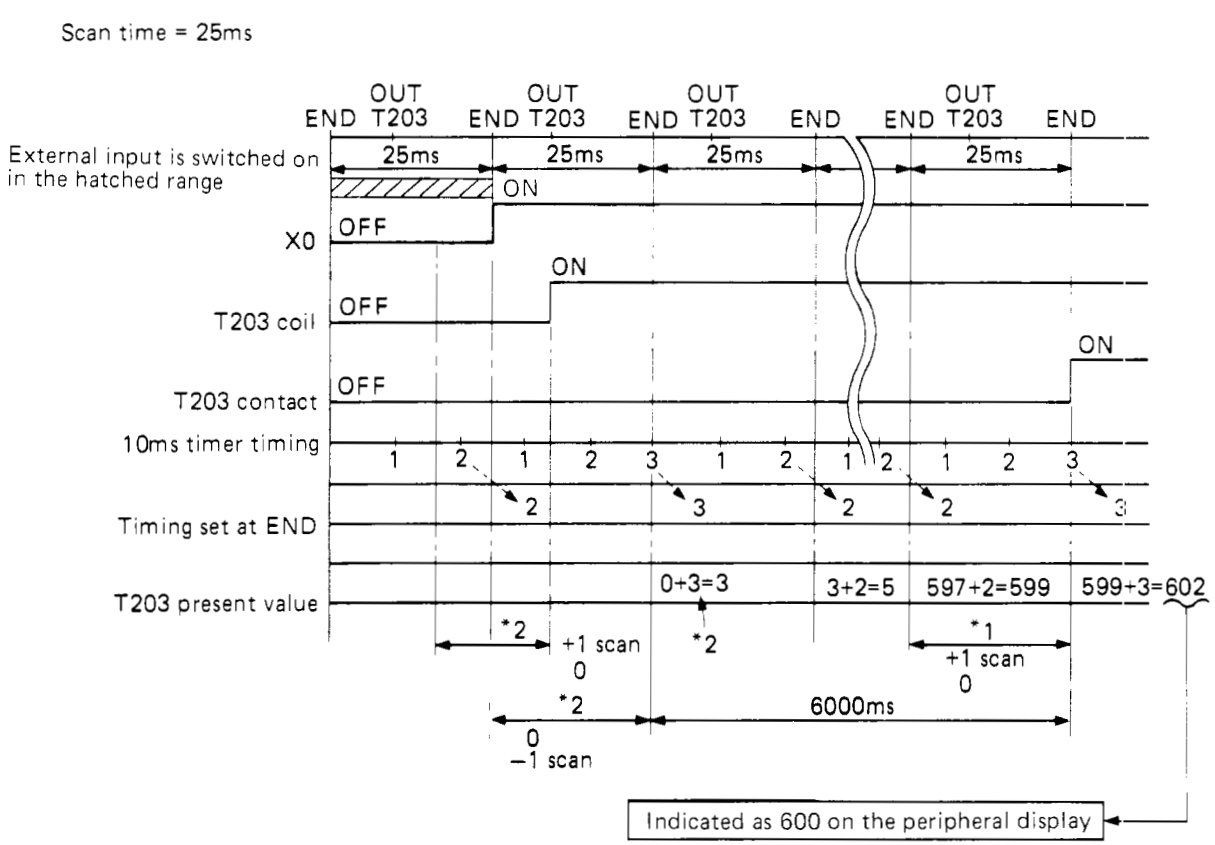


Fig. 3.3 Timer Timing

T203 time-out period includes the following errors:

*1: 10ms timer error (+1 scan time)
*2: Error depending on timing of timer input continuity and location of the OUT T□ instruction in program (±1 scan time)

A 10ms timer's accuracy is therefore +2 scan time (+0.05 seconds in Fig. 3.3).

POINT

(1) The same applies to the accuracy of a 100ms timer, i.e. +2 scan time.

(2) Contact status is updated only after the END instruction is processed, regardless of the timer coil status during any scan.

3.2.6 Maximum counting speed of normal counter

Two types of counter are available, normal and interrupt. The normal counter is used in the sequence program and the interrupt counter counts the number of interrupt signals received by the interrupt input module.
The interrupt counter can count signals which the normal counter cannot, e.g. external pulse signal inputs.
The maximum counting speed of the normal counter is described below. For the interrupt counter counting speed, see Section 3.2.15.

When a counter coil is switched on, the counter present value and contact status are updated after the execution of the END (FEND) instruction.
A counter counts the leading edges of the pulses driving its coil and counts once only when its input condition changes from off to on.

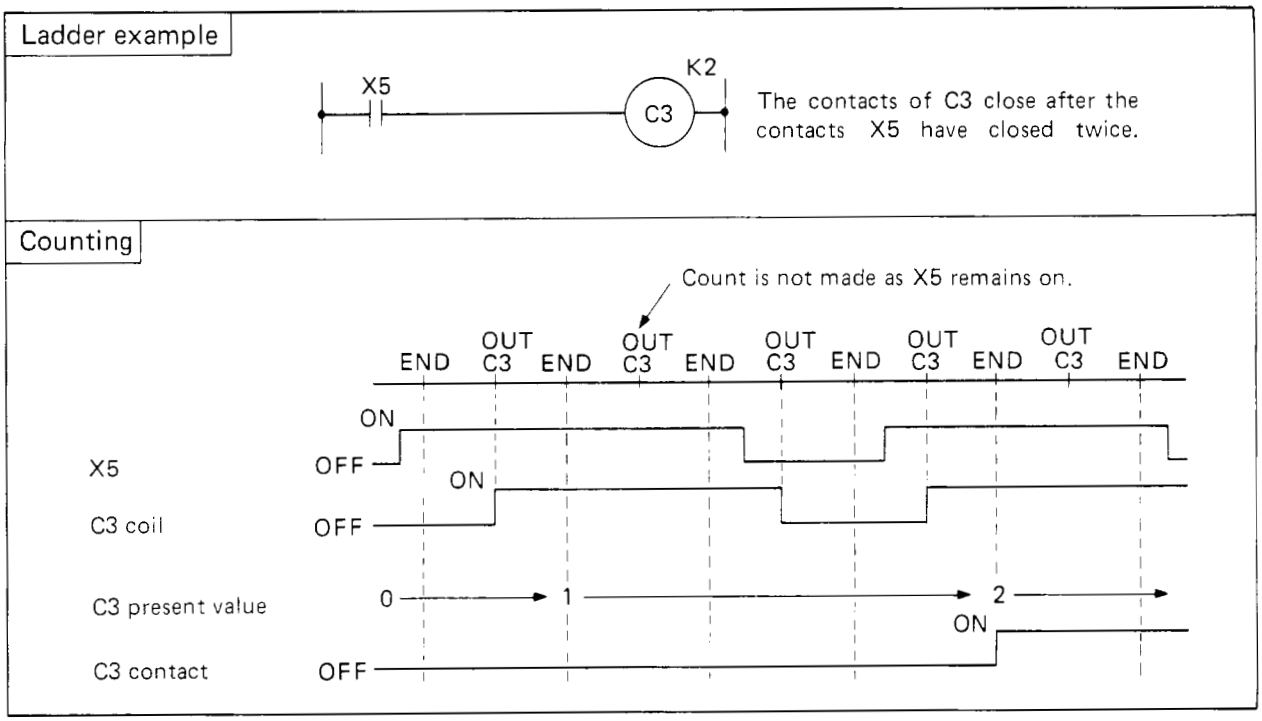


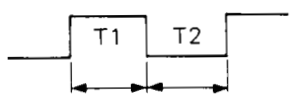
Fig. 3.4 Counter Counting

The maximum counting speed of the counter depends on the scan time. Counting is only possible if the input condition is on for more than one scan time.

$$\text{Maximum counting speed } Cmax = \frac{n}{100} \times \frac{1}{ts} \text{ (times/sec)}$$

where n = duty (%)
Duty is the ratio of the input signal's on time to off time as a percentage.

Count input signal



If $T1 \leqq T2$ $\quad n = \frac{T1}{T1 + T2} \times 100(\%)$

If $T1 > T2$ $\quad n = \frac{T2}{T1 + T2} \times 100(\%)$

ts: Program scan time (sec)

3.2.7. Self-diagnosis

Self diagnosed errors are displayed on the LEDs on the front of the CPU as ASCII messages. For information on resetting errors, see Section 7.3.

Diagnosis		CPU Status	"RUN" LED Status	Error Display
Memory error	Instruction code check	Stop	Off	INSTRCT. CODE ERR.
	Parameter check			PARAMETER ERROR
	No END instruction			MISSING END INS.
	Instruction execution disable			CAN'T EXECUTE (P)
	Instruction execution disable			CAN'T EXECUTE (I)
	No memory cassette			CASSETTE ERROR
CPU error	RAM check	Stop	Off	RAM ERROR
	Operation circuit check			OPE. CIRCUIT ERR.
	Watch dog error monitor			WDT ERROR
	Sub CPU check			SUB-CPU ERROR
	END instruction not executed			END NOT EXECUTE
	Interrupt error			MAIN CPU DOWN
I/O error	I/O unit verify	Stop / Run	Off / On	UNIT VERIFY ERR.
	Fuse blow			FUSE BREAK OFF
Special function unit error	Control bus check	Stop	Off	CONTROL-BUS ERR.
	Special function unit error			SP. UNIT DOWN
	Link unit error			LINK UNIT ERROR
	I/O interruption error			I/O INT. ERROR
	Special function unit assignment error			SP. UNIT LAY. ERR.
	Special function unit error	Stop / Run	Off / On	SP. UNIT ERROR
	Link parameter error	Run	On	LINK PARA. ERROR
Battery	Battery low	Run	On	BATTERY ERROR
*Operation check error		Stop / Run	Off / On	OPERATION ERROR

Table 3.7 Self-Diagnosis List

REMARKS

Two modes described in the "CPU Status" and "RUN LED Status" columns in Table 3.7 indicate that they can be changed by the setting of peripheral unit (GPP, HGP or PU).

Item \ Setting			Default value	Setting range	Usable Peripheral Equipment		
					A7PU	A6GPP	A6HGP
Function setting	I/O number assignment	Input (X) unit	None	I/O slots to be allocated as 16, 32, 48 or 64 point.	—	○	○
		Output (Y) unit					
		Special function unit					
		Empty slot					
	Remote run/pause control from digital input.		None	X0 to 7FF (1 point each for run and pause contacts. Setting of pause contact alone is not allowed.)	—	○	○
	Operation mode at time of error	Fuse blow	Continue	Stop/continue	—	○	○
		I/O verify error	Stop				
		Operation error	Continue				
		Special function unit check error	Stop				
	Annunciator display mode		F number display	Display of only F number or alternate display of F number and comment (Only alphanumeric characters may be displayed for comment.)	—	○	○
	STOP → RUN operating mode		Operation status prior to stop is re-output.	Output data may be re-used at beginning of new operation or cleared	—	○	○
Print title			None	An alphanumeric print out title may be added	—	○	○
Keyword entry			None	Max. 6 digits in hexadecimal (0 to 9, A to F)	○	○	○

Table 3.8 Parameter Setting Range (Continued)

REMARKS

(1) When estimating the memory cassette size required, calculate the number of bytes used from the settings made as follows:

Item	Setting Unit	Number of Bytes
Sequence program capacity	1K step	2K bytes
Subsequence program capacity		
File register capacity	1K point	2K bytes
Comment capacity	64 points	1K bytes
Sampling trace enabled	128 times	1K byte

(2) The minimum comment capacity setting is 1K bytes.

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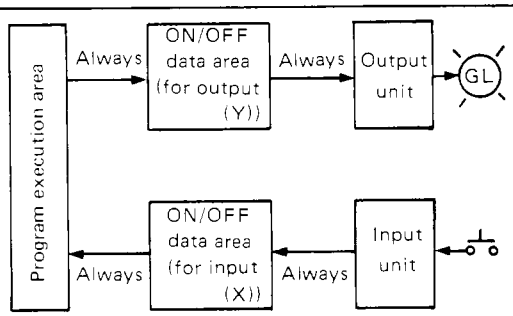
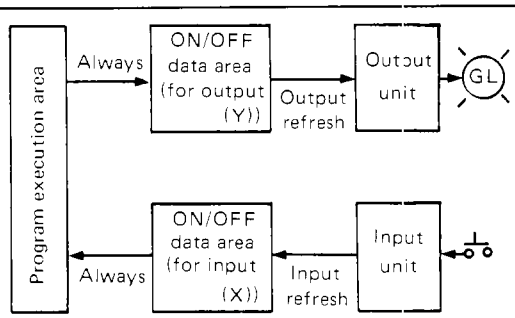
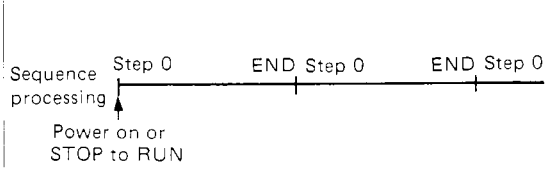
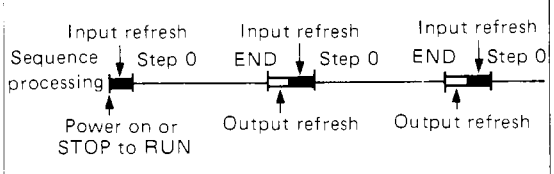
3.2.9 I/O control mode switching (direct/refresh)

The following I/O control modes are available:

1) Input and output in direct mode.
2) Input in direct mode, output in refresh mode.
3) Input in refresh mode, output in direct mode.
4) Input and output in refresh mode.

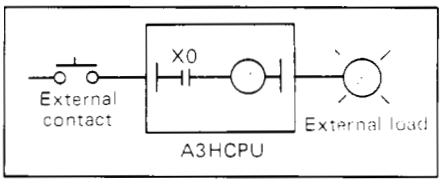
The processing of input (X) and output (Y) is different in direct and refresh modes. The processing of other devices and special function units (FROM/TO instructions) is the same in direct and refresh modes.

(1) Comparison between direct and refresh modes

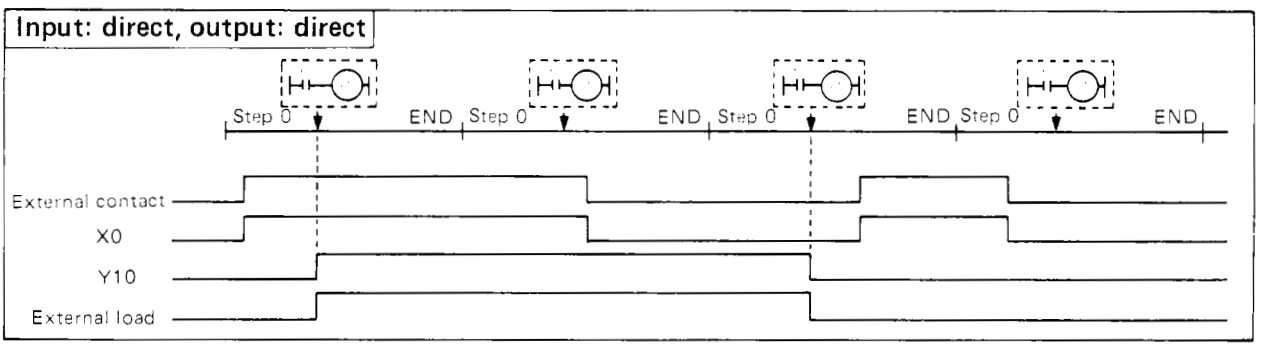
<table>
<tr><th></th><th>Direct Mode</th><th>Refresh Mode</th></tr>
<tr><td>Processing</td><td> 
</td><td> 
</td></tr>
<tr><td>Sequence processing</td><td> 
</td><td> 
</td></tr>
<tr><td>Input (X) processing</td><td>When an external contact is switched on, the ON data is immediately written to the ON/OFF data area and the corresponding device is switched on in the sequence program in the program execution area.</td><td>The ON data is transferred to the ON/OFF data area by the input refresh executed at the beginning of the next scan and the corresponding device is switched on in the sequence program in the program execution area.</td></tr>
<tr><td>Output (Y) processing</td><td>When the output (Y) is switched on in the sequence program, the ON data is immediately transmitted from the ON/OFF data area to the output unit and the external load is switched on.
The contact with the same number in the program is also switched on immediately.</td><td>When the output (Y) is switched on in the sequence program, the ON data is stored in the ON/OFF data area until the current program scan is complete. When the output refresh is executed after the END instruction, the data is transmitted to the output unit and the external load switched on.
In this case, the contact with the same number in the program is switched on immediately after the output (Y) coil is switched on.</td></tr>
</table>

(2) I/O timing

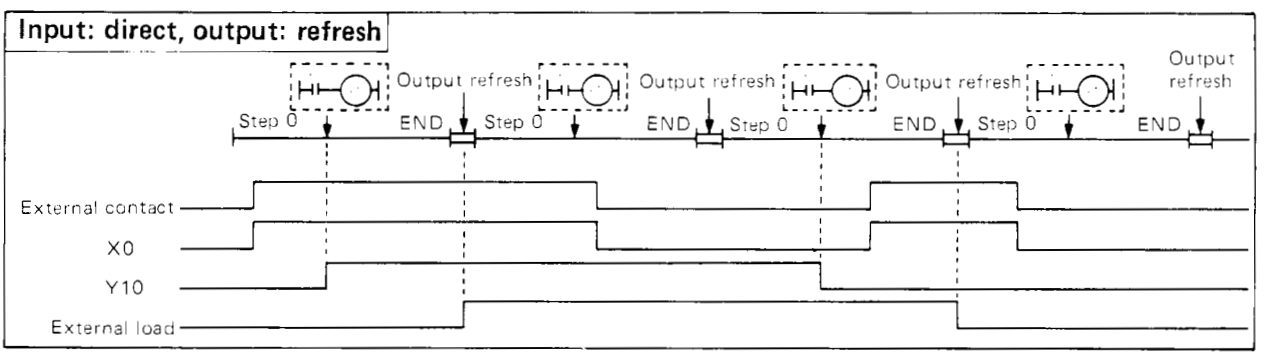
The ON/OFF timings of input (X), output (Y) and external load differ as shown below in direct and refresh modes.



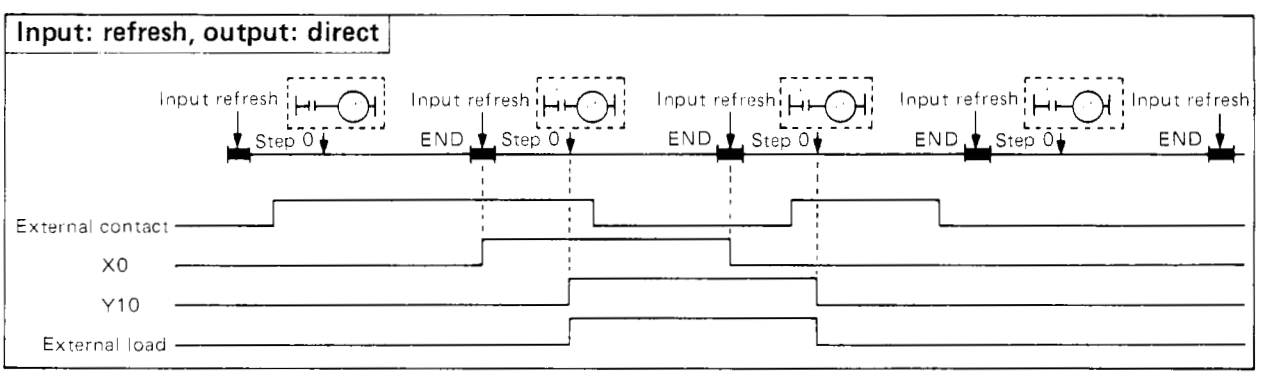
Input: direct, output: direct



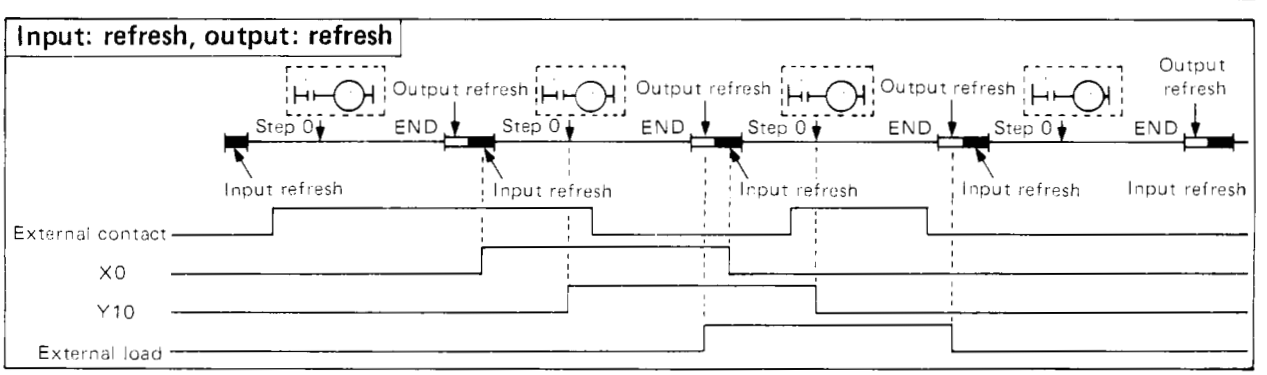
Input: direct, output: refresh



Input: refresh, output: direct



Input: refresh, output: refresh

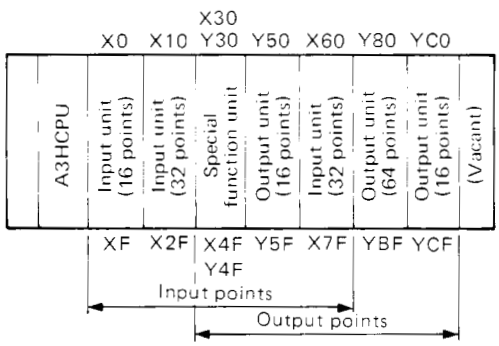


(3) I/O refresh time

Instructions applying to inputs (X) and outputs (Y) are processed faster in refresh mode than in direct mode because the physical inputs and outpus are not processed during the scan.
In this case, the program scan time is longer by the refresh time than the actual program execution time since inputs and outputs must be refreshed after the END instruction.
The refresh time can be calculated as follows:

$$\text{Refresh time} = \frac{\text{number of input + output points}}{16} \times 4.375\ (\mu\text{sec})$$

The number of input and output points depends on the I/O unit and special function unit locations as shown below.



POINT

The special function unit is calculated as having 32 inputs and 32 outputs.
Example: X30 to X4F, Y30 to Y4F

The number of input points is the sum of the I/O points of all units from the input or special function unit in the lowest slot number to the one in the highest slot number.

Example: Sum of the input points between X0 and X7F in the above I/O allocation

Input points = 16 + 32 + 32 + 16 + 32 = 128

The number of output points is the sum of the I/O points of all units from the output or special function unit in the lowest slot number to the one in the highest slot number.

Example: Sum of the unit points between Y30 and YCF in the above I/O allocation

Output points = 32 + 16 + 32 + 64 + 16 = 160

Calculation of refresh time

Refresh time can be reduced by arranging the same units sequentially as shown in Fig. 3.5.

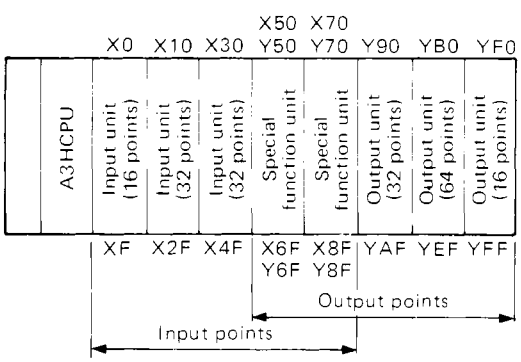


Fig. 3.5 Same Units Loaded Sequentially

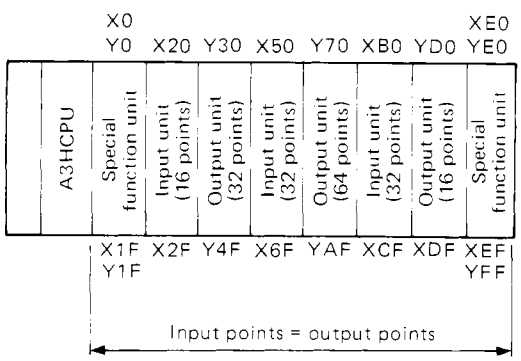

X0 XE0
Y0 X20 Y30 X50 Y70 XB0 YD0 YE0
A3HCPU
Special function unit
Input unit (16 points)
Output unit (32 points)
Input unit (32 points)
Output unit (64 points)
Input unit (32 points)
Output unit (16 points)
Special function unit
X1F X2F Y4F X6F YAF XCF XDF XEF
Y1F YFF
Input points = output points

Fig. 3.6 Same Units Loaded Non-sequentially

Calculation of refresh time in Fig. 3.5

Input points = 16 + 32 + 32 + 32 + 32 = 144
Output points = 32 + 32 + 32 + 64 +16 = 176

$\therefore$ Hence, refresh time = $\frac{144 + 176}{16}$ x 4.375 = 87.5 (μsec)

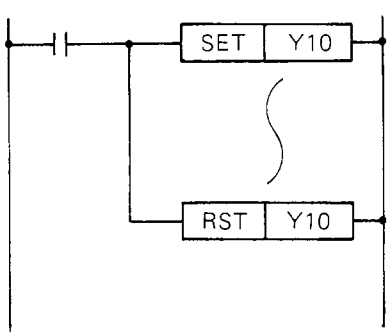
Calculation of refresh time in Fig. 3.6

Input points = output points = 32 + 16 + 32 + 32 + 64 + 32 + 16 + 32 = 256

$\therefore$ Hence, refresh time = $\frac{235 + 256}{16}$ x 4.375 = 140 (μsec)

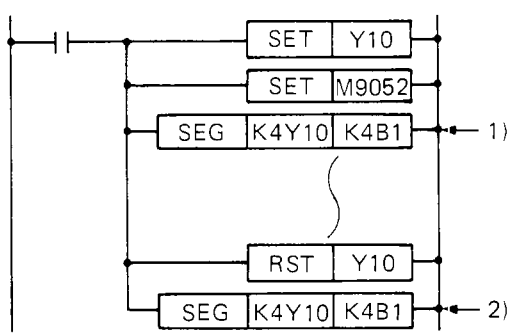
(4) Notes on refresh mode

1) In refresh mode outputs (Y) cannot be switched on and off within the same scan as shown in Fig. 3.7. In this case, the instruction at the higher step number takes priority.
This problem can be overcome by using the partial refresh instruction as shown in Fig. 3.8.



In this case, Y10 is switched on in the sequence program after the SET instruction is executed and remains on until the RST instruction is executed and the output refresh only uses the final (off) data to control the output hardware.

Fig. 3.7

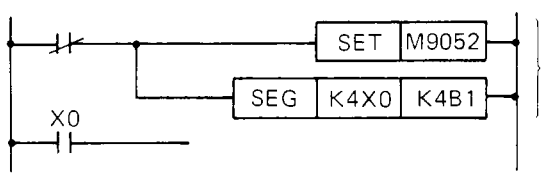


SET M9052 switches the SEG instruction to the partial refresh instruction.
Y10 ON data is transmitted to the output unit by the partial refresh instruction 1).
Y10 OFF data is transmitted to the output unit by the partial refresh instruction 2).

For details on the SEG instruction, see Appendix 1.

Fig. 3.8

2) When refresh mode has been selected for inputs (X), the input hardware must remain on or off for a least one scan as input signals are all entered at the beginning of the scan. The inputs (X) in the sequence program remain unchanged if the input hardware is switched on then off again within one scan.
Any input signal must be read using the partial refresh instruction as shown in Fig. 3.9 if it is being switched on-off-on or off-on-off within one scan.



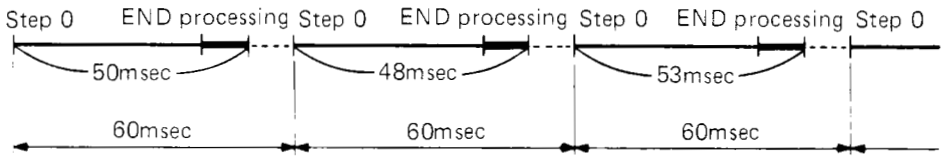
Reads external input signal ON/OFF state using partial refresh instruction.

For details on the SEG instruction, see Appendix 1.

Fig. 3.9

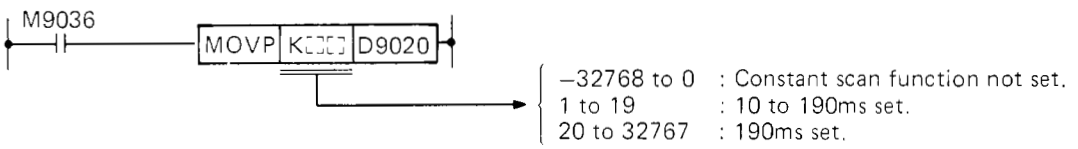
3.2.10 Constant scan

Executes the program repeatedly at a specified interval as shown below.



(1) The constant scan period can be set between 10ms and 190ms in 10ms increments.

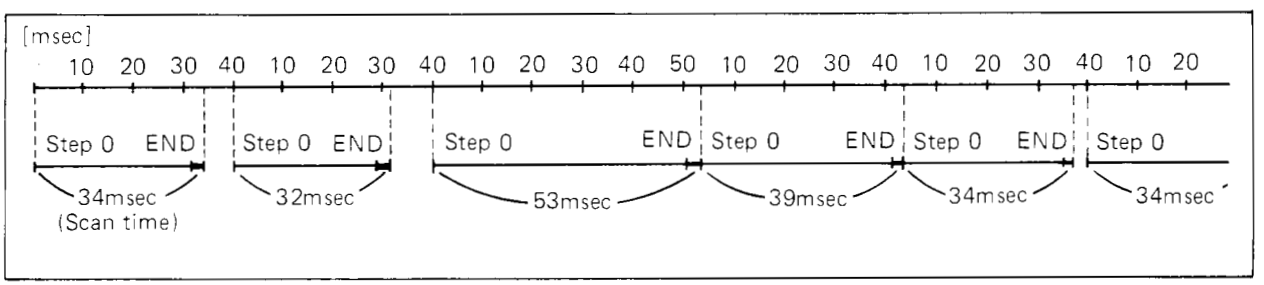
(2) The set value is written to special data register D9020.



POINT

The ladder rung shown above should be written at the beginning of the sequence program since D9020 is cleared to 0 when the PC is switched on or reset.

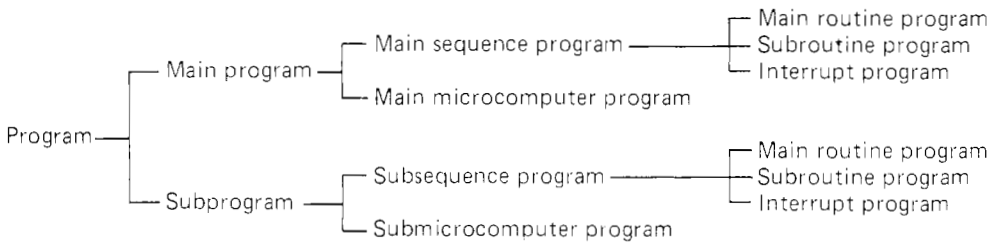
(3) The constant scan period is ignored if the sequence program scan time is greater than the set value.
The constant scan facility may not operate normally if the scan time becomes temporarily greater than the set value, since the constant scan function is processed by the A3HCPU timers. The set value must therefore be specified with the maximum program scan time fully taken into consideration. (See below)



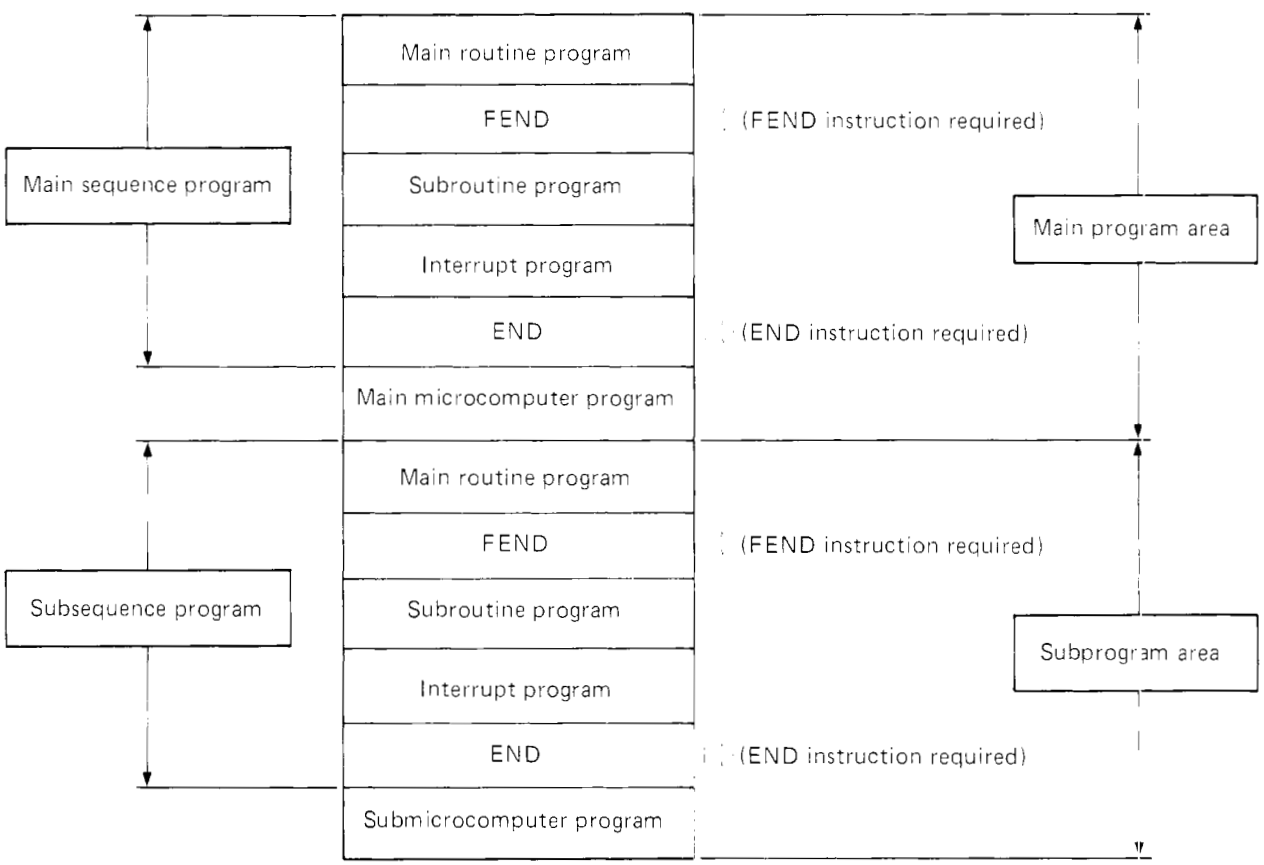
(4) The sequence program is not processed after the END instruction until the next scan is started. (All device memory data remains as it was before the END instruction was processed.) An interrupt program, however, will be executed if its start factor occurs during the wait period prior to the next scan.

3.2.11 Program types

The following types of program are available on the PC.



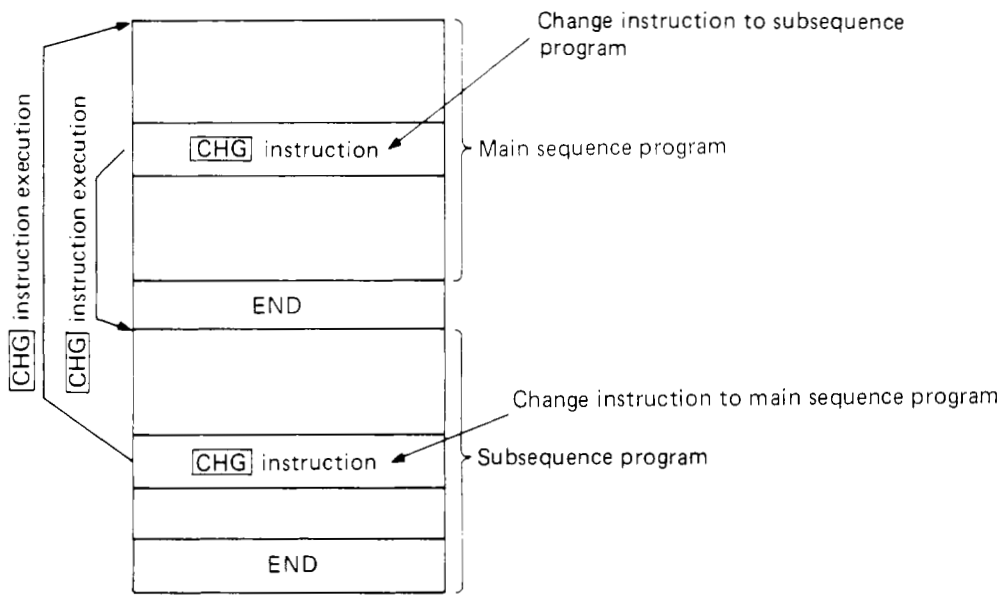
Programs are written in the user memory area as shown below.



The subsequence, interrupt, subroutine and microcomputer programs are explained in the following pages.

3.2.12 Subsequence program

The subsequence program allows a program of up to 30K steps to be written in a program area separately from that of the main sequence program.
Therefore, two programs (main sequence program and subsequence program) can be run alternately in series or either program can be separately selected and run.
The [CHG] instruction is used to switch between main and subsequence programs. After entering a main or subsequence program, that program is processed repeatedly until the [CHG] instruction is executed again.



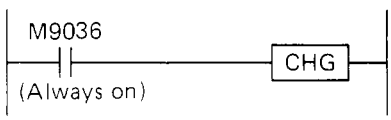
When the [CHG] instruction is executed, the operating system operates the END processing routine (renewal of present value of T/C, self-diagnosis, WDT reset) before the program pointer jumps to the other program area.

[REMARKS]

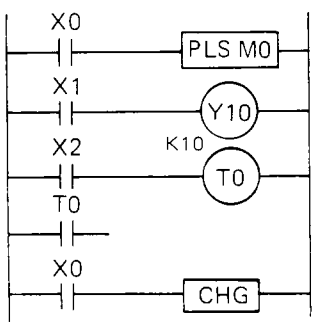
Typical applications for a subsequence program are as follows: 1) By entering the [CHG] instruction in front of the END instruction the programs switch repeatedly between main and subsequence programs giving, in effect, a 60K-step program. 2) By writing the same program in both the sequence and subsequence program areas, program modifications may be made to one area while the other area is running without the risk of affecting the controlled operation.

3.2.13 Notes on writing subsequence programs

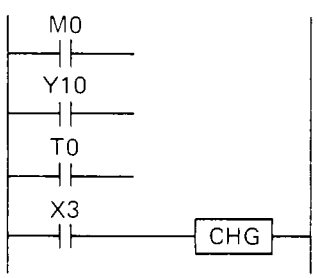
(1) The CHG instruction is executed continuously while its condition contact is on. The following program should be written in front of the END instructions in the main and subsequence programs to run the two alternately.



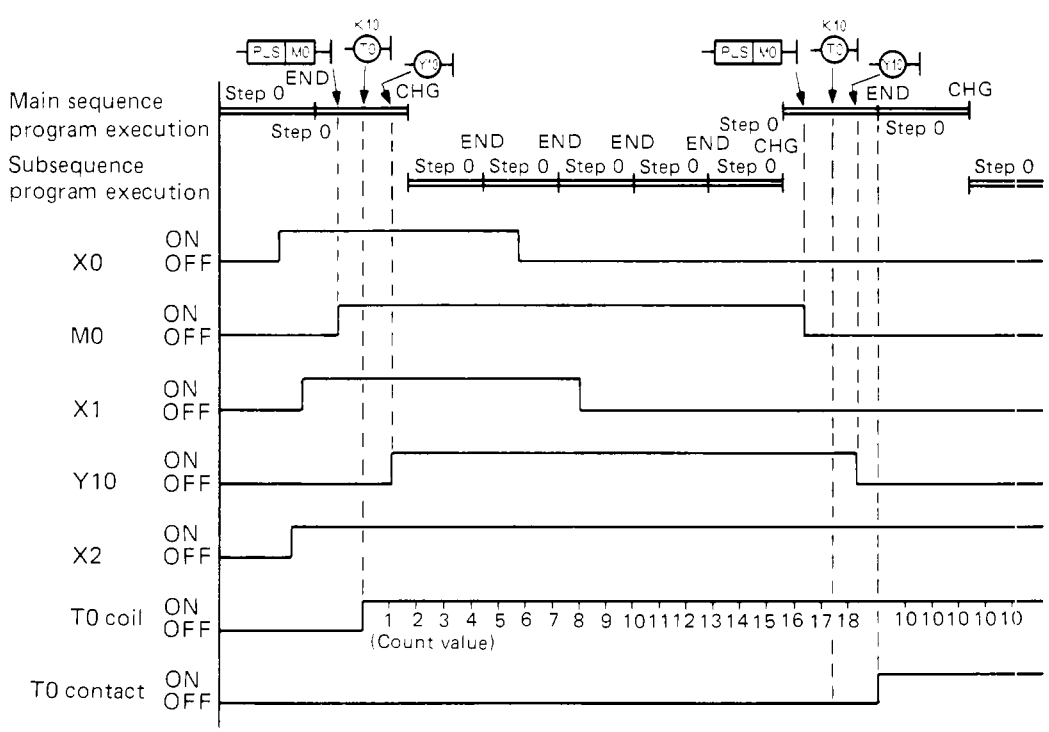
(2) The state of each device in one program area will remain unchanged when the other program area is being run (assuming the device is only controlled in one program area). The following example illustrates the effect of running a subsequence program for a given number of scans after the main program has run for one scan.



Main sequence program



Subsequence program

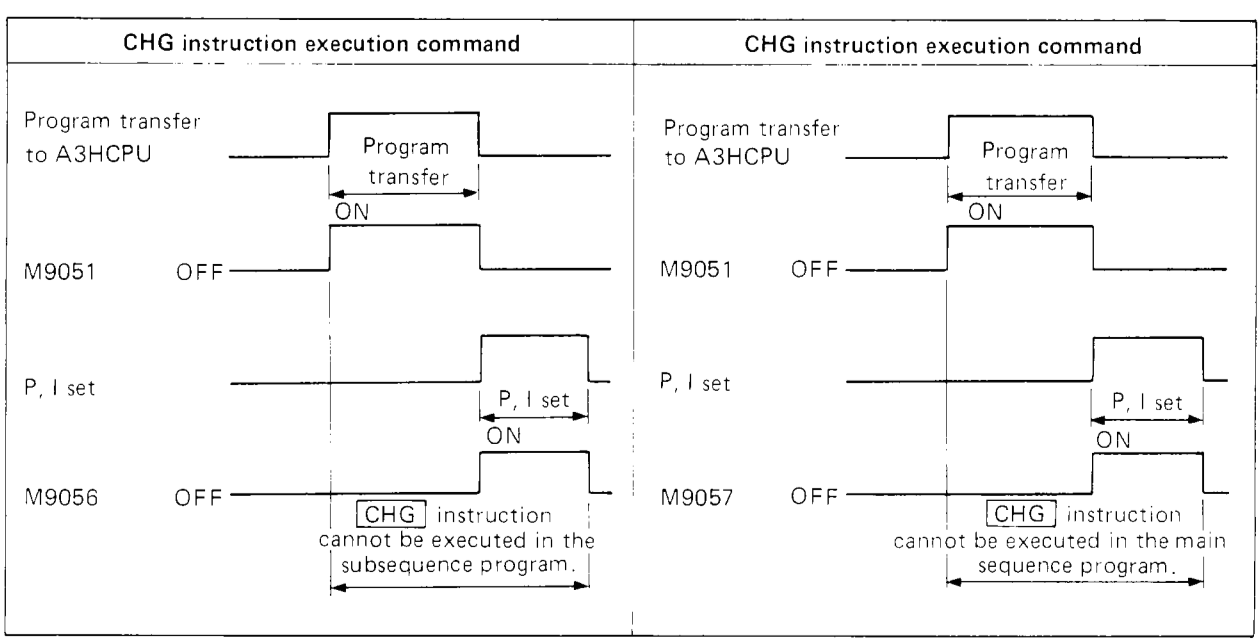


Therefore, for this type of application, avoid using the contacts of a device when its coil is addressed in the other program area.
Some areas of the main and subsequence program may need to be identical in order to avoid these problems.

(3) Sub (or main) sequence program rewrite during main (or sub) sequence program operation

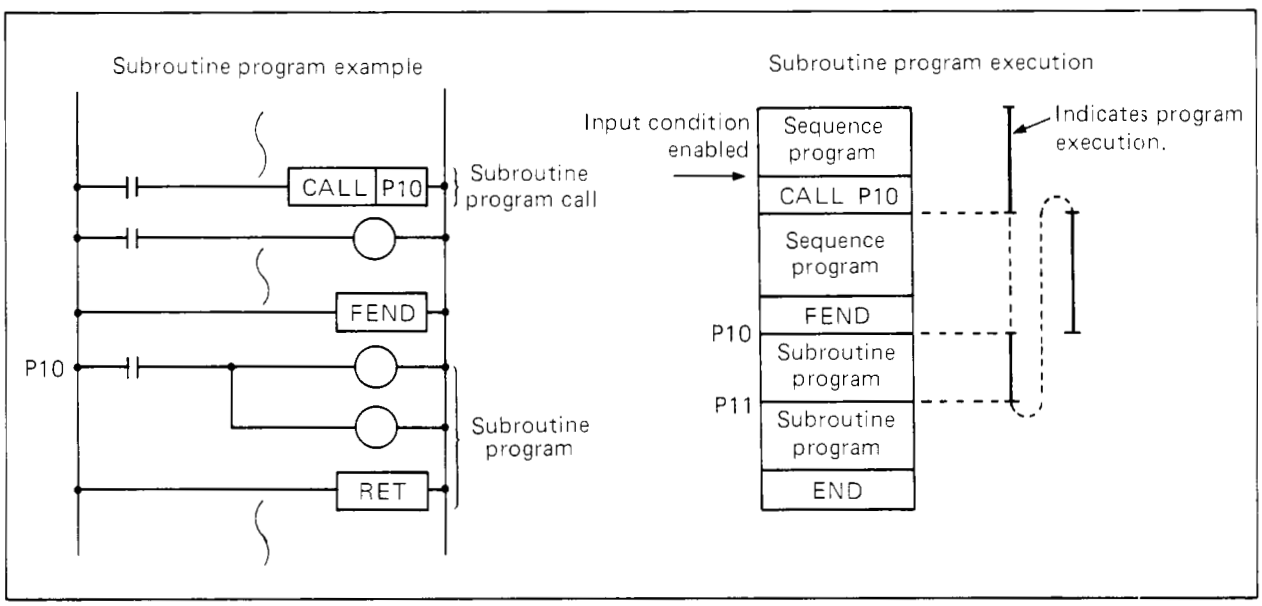
Programs may be written to a sub or main program area while the PC is running that program area, however, in some cases control problems may occur (for example WDT time out). In order to avoid this it is preferable to write a program into whichever program area, sub or main, is currently not running. In this case, the CHG instruction may be disabled using special relays M9051, M9056 and M9057.

	Main Sequence Program	Sub Sequence Program
Ladder example	CHG instruction execution command M9051 M9057 CHG	CHG instruction execution command M9051 M9056 CHG
Operation	The CHG instruction is executed and the main sequence program switched to the subsequence program. The CHG instruction is not executed when M9051 and/or M9057 is on.	The CHG instruction is executed and the sub-sequence program switched to the main sequence program. The CHG instruction is not executed when M9051 and/or M9056 is on.
Special relays	M9051 . . .Switched on during main sequence program transfer to the A3HCPU. M9056 . . .Switched on on completion of the main sequence program transfer to the A3HCPU. Switched off on completion of pointer (P) or interrupt pointer (I) address storage. M9057 . . .Switched on on completion of the subsequence program transfer to the A3HCPU. Switched off on completion of pointer (P) or interrupt pointer (I) address storage.	

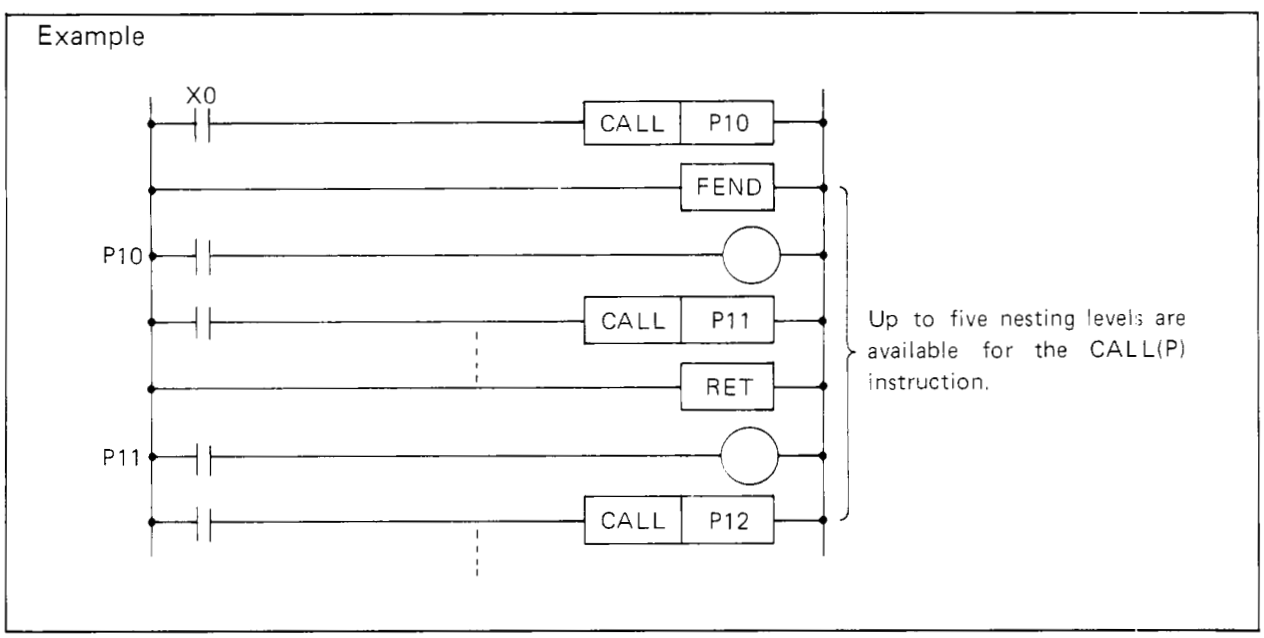


3.2.14 Subroutine program

Used to call a common program routine several times during a scan or when a given condition is enabled. The subroutine program must be written after the sequence program (after FEND) and is called by the CALL instruction. When the input condition for the CALL instruction is on, the subroutine is run, when it is off, the sequence program is run.



Up to five subroutine nesting levels are possible.



3.2.15 Interrupt program and interrupt counter

Interrupt signals may be given to the PC CPU via the AI61 interruption input module. Each input point on this module corresponds to an interrupt pointer I0 to I15.
Interrupt pointers may be individually designated as interrupt program pointers or interrupt counters in the PC parameters.
If designated as an interrupt program pointer, the specified program area is run when its interrupt signal is received.
If designated as an interrupt counter, the specified counter is incremented each time its interrupt signal is received.

POINT

Each interrupt pointer may be associated with either an interrupt program or an interrupt counter but not both. Do not write interrupt programs to interrupt pointers which have a counter assigned to them in the parameters.

(1) Interrupt pointers (I)

Interrupt pointers (I) are assigned to interrupt factors as shown below:

Interrupt Pointer	Interrupt Factor		Interrupt Pointer	Interrupt Factor	
I0	From AI61 interrupt input module	1st point	I16	(*1) Interrupt generated by special function unit	1st unit
I1		2ndpoint	I17		2nd unit
I2		3rd point	I18		3rd unit
I3		4th point	I19		4th unit
I4		5th point	I20		5th unit
I5		6th point	I21		6th unit
I6		7th point	I22		7th unit
I7		8th point	I23		8th unit
I8		9th point	I24	Unused	
I9		10th point	I25		
I10		11th point	I26		
I11		12th point	I27		
I12		13th point	I28		
I13		14th point	I29	Interrupt factor every 40ms of internal timer (*2)	
I14		15th point	I30	Interrupt factor every 20ms of internal timer (*2)	
I15		16th point	I31	Interrupt factor every 10ms of internal timer (*2)	

(a) *1 Interrupt pointers I16 to I23 are dedicated to interrupt signals generated by special function units (not AI61)
Pointers are assigned to modules in order of I/O allocation.

(b) *2 Interrupt pointers I29 to I31 are time based interrupts at intervals of 40ms, 20ms and 10ms in which the interrupt program or count is executed at the specified intervals.

(c) The interrupt priority is as follows:

High —— I16 ~ I23, I0 ~ I15, I31, I30, I29 (Priority) ——→ Low

POINT

(1) The EI instruction should be written in the program to enable interrupt processing. Any interrupt factor occurring prior to the EI instruction will wait to be processed until the EI instruction is processed. Any interrupt occurring while the PC is in STOP mode will wait to be processed unitl after the PC is in RUN mode and the EI instruction has been processed.

(2) Any interrupt program may be run during the execution of basic or application instructions.

(2) Interrupt program

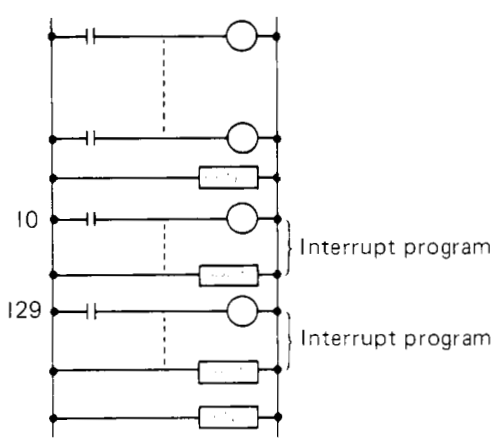
The interrupt program is executed when its interrupt factor occurs and is written to any of the interrupt pointers I0 to I31.

(a) The interrupt program must be written after the FEND and before the END instructions.

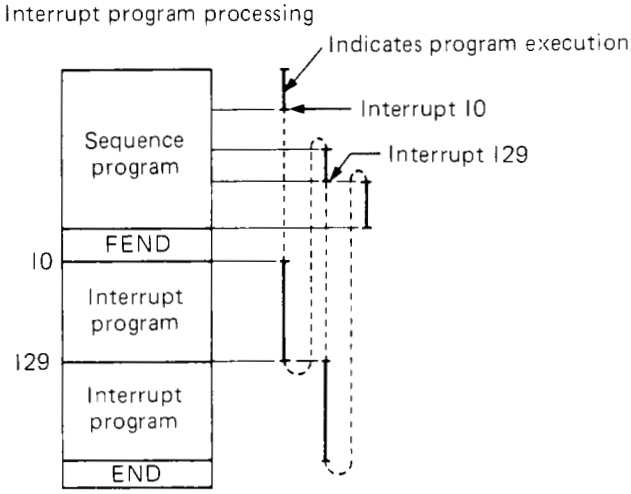
(b) The interrupt pointer (I) must be written at the beginning of the interrupt program.

(c) The IRET instruction must be written at the end of each interrupt program in order to return to the sequence program location from which the jump was made to the interrupt program.

Interrupt program example



Interrupt program processing



Example: The END processing time is 2ms. If the max. instruction processing time is 0.3ms, a program is not written during run, there is no interrupt program, and two interrupt counters are used.

$$\text{Max. counting speed} = \frac{1}{(0.002 + 0.0005 \times 2)\ (\text{sec})} = \text{approx. 333 Pulse/sec.}$$

Hence, the highest speed pulse train which may be reliably read by the A3HCPU, with the above conditions is 333 pulse/sec.

POINT

(1) The interrupt counters may miss counts depending on the timings of the END processing and the pulse signal if a pulse signal of more than 333PPS is input in the above example.

(2) The sequence program cannot be executed and a "WDT ERROR" will occur if too many interrupt counters are used. In this case, the number of interrupt counters must be reduced or the input pulse counting speed decreased. The occurrence of this will also depend on other factors in the PC program, especially scan time.

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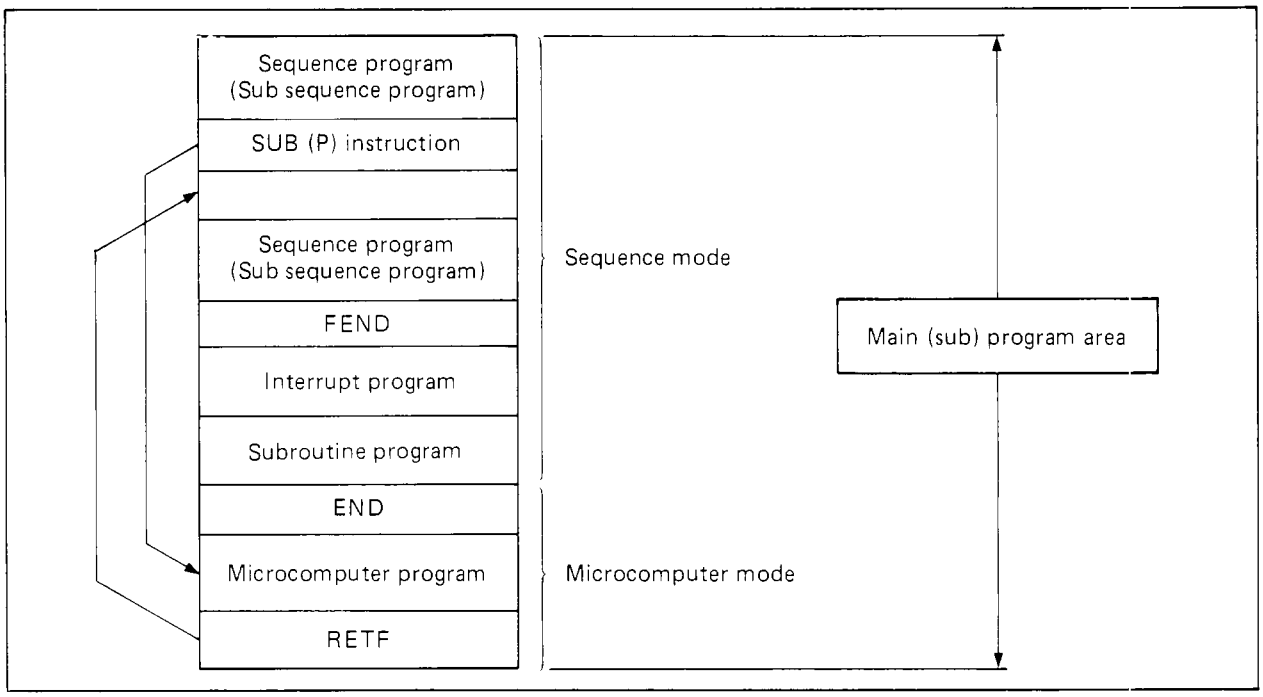
3.2.16 Microcomputer program

Programs written in machine language located in the micro computer program area of the user memory, may be called and run during sequence program processing.



Calling a microcomputer program

(1) Microcomputer mode specifications

Item	Specifications
CPU	80286 (8MHz)
Microcomputer program area	Uses the main (sub) program area. Memory capacity is as follows: 0 to 58K bytes (in 2K byte increments) Relation between the main (sub), sequence and microcomputer programs is as follows: (Main (sub) program memory capacity) = (sequence program memory capacity) + (microcomputer program memory capacity)
Work area	A100H to A1FFH (256 bytes) (Built in the A3HCPU)
Stack	User area: 128 bytes
Instructions unavailable from 80286	INT, INTO, IRET, IN, OUT, HLT, WAIT, LOCK, ESC, CLI, STI
Mode	Use 80286 Real mode only

(2) Notes on writing microcomputer programs

1) The register used must be protected before the microcomputer program is executed and must be unprotected when execution goes back to the sequence program.
2) The microcomputer program is only executed when called by the SUB (P) instruction in the sequence program.
3) The RETF instruction (outside the segment) must be used to switch from the microcomputer program back to the sequence program.

3.2.17 Status latch

Used as a fault finding facility, this enables a "snap shot" of the PC device memory to be taken and stored in a dedicated area of the PC memory. The snap shot is triggered by the SLT instruction which is written in the same way as a coil type device.
The instruction should be written into the program so that it is activated by the series of contacts and / or conditions which need investigation.
The snap shot is examined using the GPP/PHP/HGP to read out the data from the PC memory and then monitor it.
The following data may be written to the status latch memory area:

(1) Device memories

X, Y, M, L, S, F, B, T/C contact, coil ..... ON/OFF data.
T, C ..... Present value.
D, W, A, Z, V ..... 16-bit data.

(2) File registers (R)

16-bit data

3.2.18 Sampling trace

Used as a fault finding facility, this allows the data from a selection of specified devices to be recorded in a dedicated area of the PC memory for each of a defined number of scans or at defined time intervals. This allows the recorded progress of device statuses to be examined over a series of scans or time intervals.
The sampling trace is triggered by the STRA instruction which is written in the same way as a coil type device.
The instruction should be written into the program so that it is activated by the series of contacts and / or conditions which need investigation.
The sampled data is examined using the GPP/PHP/HGP to read out the data from the PC memory and then monitor it.
The number of devices which may be set up for the sampling trace is limited as follows.

Bit devices (X, Y, M, L, S, F, B, T/C contact, coil) ..... Max. 8 points
Word devices (D, W, R, A, Z, V, T/C present value) ..... Max. 3 points

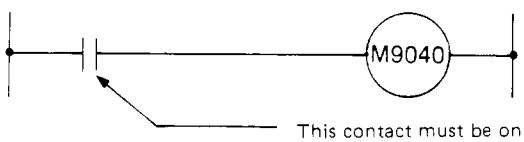
3.2.19 Pause function

The PAUSE function allows program processing to be stopped while maintaining the outputs in the state that they were immediately prior to entering PAUSE. (Including analog outputs)

(1) Entering Pause status

Pause status may be entered in either of two ways.

(a) Pause status may be set by moving the CPU keyswitch to the "PAUSE" position.
The coil of special relay M9040 must be switched on to enable the pause facility. Either the CPU keyswitch or special relay M9040 may be switched first, the pause facility will be set in both cases when the other condition is met.
Pause status cannot be set unless M9040 is on.



(b) Pause status may be set by switching on an input as defined in the PC parameters.
The coil of special relay M9040 must be switched on to enable the pause facility. Either the remote pause input or special relay M9040 may be switched on first, the pause facility will be set in both cases when the other condition is met.
Any input (X), which has been assigned as the remote pause contact, will be valid even if it does not appear in the sequence program.
The remote pause input is valid when the CPU is in RUN or STEP RUN mode.
For details on allocating an input to remote pause control, refer to the relevant peripheral operating manual (GPP/PHP/HGP).

(c) Pause status may be set from the GPP/PHP/HGP by selecting REMOTE PAUSE in PC TEST mode and pressing [GO]. Pause status is reset by repeating the operation.

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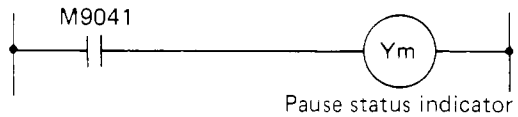
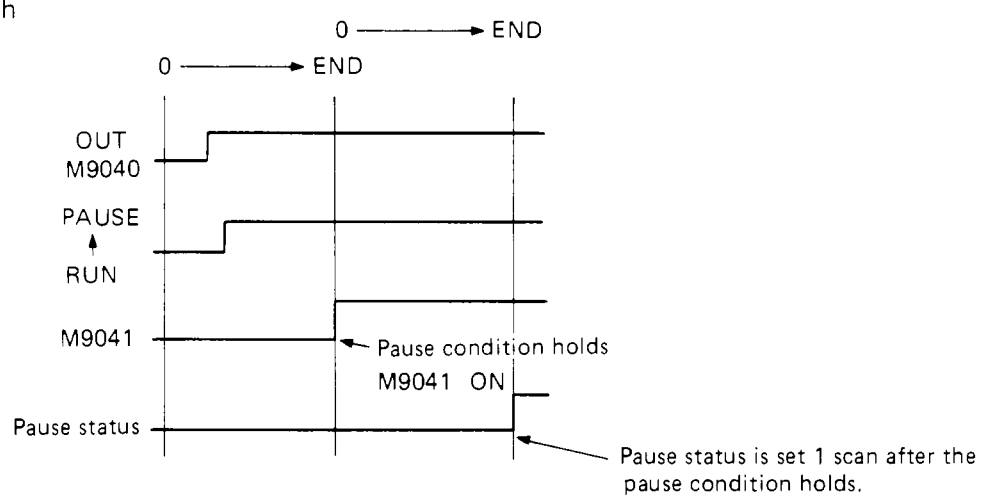
(2) Use of special relay M9041

M9041 is switched on when the PC is in pause status. It may be used to provide external indication that the PC is in pause status as in the example below.

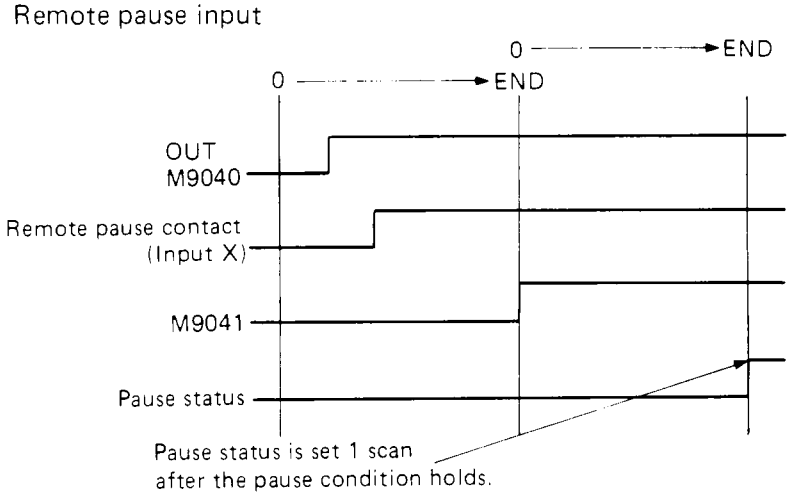


(3) Pause status timing chart

(a) CPU keyswitch



(b) Remote pause input



The RUN LED is off during pause status.

3.2.20 Step run

This is a fault finding facility which allows the program to be run step by step or scan by scan. Step run is controlled from the GPP/PHP/HGP which simmultaneously monitors devices and the PC CPUs operating condition.

3.2.21 Remote run

The remote run facility allows the PC's run/stop status to be controlled via an input as defined in the PC parameters. When the PC is in run mode and the specified input is switched on, the PC switches to stop mode. When the specified input is switched off, the PC returns to run moce.
Any input (X) which has been assigned as the remote pause contact, will be valid even if it does not appear in the sequence program.
The remote run input is valid when the CPU is in RUN, STEP RUN or PAUSE mode.
For details on allocating an input to remote run control, refer to the relevant peripheral operating manual. (GPP, PHP or HGP)
Run status may also be set from the GPP/PHP/HGP by selecting REMOTE RUN in PC TEST mode and pressing GO .

3.2.22 Assignment of I/O numbers

Where neccessary, the I/O assignment may be set up in the PC parameters. Where this is not required, the parameter "I/O assignment" table in the parameters should be left blank and the PC will use the actual physical I/O assignment according to the I/O units located in its base(s).

I/O assignment allows the following:

1) Vacant I/O slots can be ignored and those I/O points not wasted. (an empty I/O slot would otherwise use up 16 I/O points)

2) A vacant slot may be reserved for future system expansion by assigning 16, 32, 48 or 64 I/O points to it.
This means that subsequent system expansion will not require I/O address changes.

3) I/O numbers do not change when an I/O module is removed.
(Removal of a 32 way card without parameter I/O assignment, for example, would shift all subsequent I/O numbers down by 16)

I/O assignment is optional.
I/O addresses must be calculated as follows according to whether I/O assignment has been made or not.

(1) No parameter I/O assignment

(a) Assign I/O numbers in order of extension base stage setting numbers (as opposed to order of extension cable connection.)
(b) Assign I/O numbers to the main base and extension base(s) on the assumption that each base has 8 slots. (The final 3 slots on a 5 slot base must be accounted for and represent empty I/O slots.)
(c) Assign 16 points to an empty slot.
(d) Any extension stage which has been skipped must be accounted for as 8 vacant slots.

(2) "I/O ASSIGNMENT" has been made

(a) 16, 32, 48 or 64 inputs, outputs, vacancies (i.e. a reservation for later expansion) or special function unit I/O points can be assigned to each I/O slot.

(b) A special function unit will not operate correctly if it is located in a slot allocated to the wrong type of module (i.e. X or Y) or if the I/O count is wrong.

(c) Any slot for which an I/O setting has not been made uses the actual I/O capacity of the unit loaded.

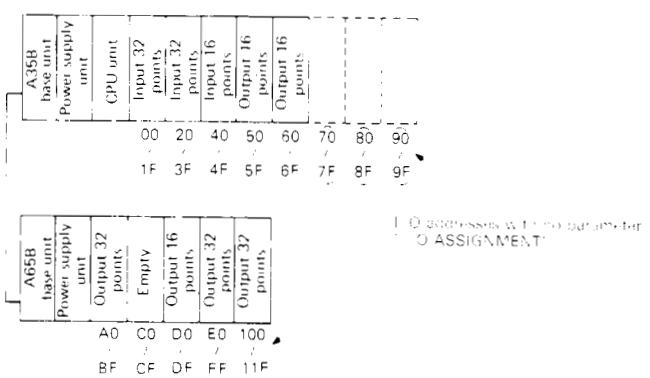
(d) The parameter I/O allocation takes priority over the actual modules I/O capacity.

Hence: The second 16 I/O points of a 32 way module placed in a slot with 16 points allocated, will be unusable, and,
The second 16 I/O points in a slot with 32 points allocated but containing a 16 way module will be unusable.

(e) Any I/O unit located in a slot allocated as vacant, cannot be used.

The following example shows the I/O addresses in a system without I/O assignment, as can be seen 16 x 4 = 64 I/O points have been wasted.

Actual loading status



I/O addresses when no parameter I/O ASSIGNMENT

The following I/O assignment for the previous system will illustrate

(1) I/O assignment

* I/O ASSIGNMENT *

SLT NO.	I/O UNT	SLT NO.	I/O UNT	SLT NO.	I/O UNT	SLT NO.	I/O UNT	SLT NO.	I/O UNT	SLT NO.	I/O UNT	SLT NO.	I/O UNT
0	X32	16		32		48		64		80		96	112
1	X32	17		33		49		65		81		97	113
2	X16	18		34		50		66		82		98	114
3	Y16	19		35		51		67		83		99	115
4	Y16	20		36		52		68		84		100	116
5	S 0	21		37		53		69		85		101	117
6	S 0	22		38		54		70		86		102	118
7	S 0	23		39		55		71		87		103	119
8	Y32	24		40		56		72		88		104	120
9	S32	25		41		57		73		89		105	121
10	Y16	26		42		58		74		90		106	122
11	Y32	27		43		59		75		91		107	123
12	Y32	28		44		60		76		92		108	124
13		29		45		61		77		93		109	125
14		30		46		62		78		94		110	126
15		31		47		63		79		95		111	127

VACANCY (S) 1 0POINT
2 16POINTS
3 32POINTS
4 48POINTS
5 64POINTS
X (X) 6 16POINTS
7 32POINTS
8 48POINTS
9 64POINTS
Y (Y) A 16POINTS
B 32POINTS
C 48POINTS
D 64POINTS
S-UNIT (F) E 16POINTS
F 32POINTS
G 48POINTS
H 64POINTS

PRESS (END) WHEN SET

MEMORY TOTAL 16K BYTES

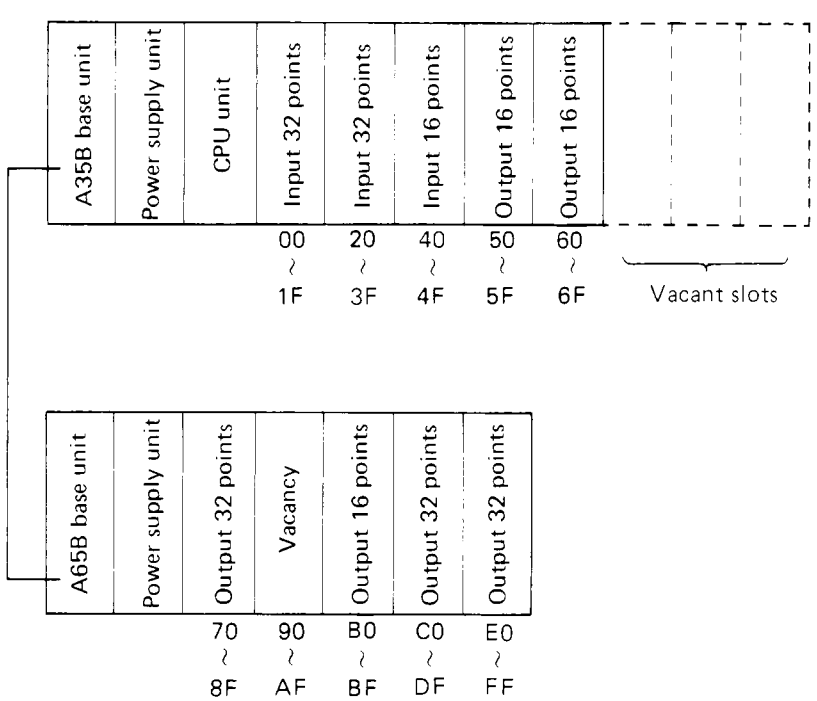
MODE PARAMETER FUNCTION

[KEY-IN DATA]

MESSAGE

[BC] A3H [GPP]

(2) I/O addresses after making "I/O ASSIGNMENT":



3.2.23 Entry code

The entry code is a security number attached to the PC program and incorperated in the PC parameters. It allows unauthorized access to the program memory to be prohibited by preventing the program from being read out of the PC or from being overwritten. Access to the program can only be gained by entering the correct entry code into the peripheral unit parameter area.
Up to 6 hexadecimal digits may be used as an entry code.
Entry codes cannot be read from the PC memory and, if forgotten, the only means of access to the PC is to first wipe the entire memory contents. (In this case all programs etc. are permanently removed from the PC memory)
Entry code handling and PC memory clearing are covered in the relevant peripheral unit operating manual.

3.2.24 Print title entry

A print out title may be permanently associated with the PC program by selecting "PRINT TITLE" from the GPP/PHP/HGP parameter menu and entering a 128 character (alphanumeric and symbol) text. This print out title is stored in the PC parameter area.
For full details refer to the relevant peripheral unit operating manual (not for A7PU)

3.3 Power Supply Unit Specifications

3.3.1 Power supply unit specifications

Table 3.9 shows the specifications of power supply units.

Item		Specifications				
		A61P	*A62P	A63P	A65P	A66P
Location in base unit		Power supply unit slot	Power supply unit slot	Power supply unit slot	Power supply unit slot	I/O unit slot
Input voltage		100–120V AC +10%, –15% (85 to 132V AC) 200–240V AC +10%, –15% (170 to 264V AC)	100–120V AC +10%, –15% (85 to 132V AC) 200–240V AC +10%, –15% (170 to 264V AC)	24V DC +30%, –35% (15.6 to 31.2 V DC)	100- 120V AC +10%, –15% (85 to 132V AC) 200- 240V AC +10% –15% (170 to 264V AC)	100–120V AC +10%, –15% (85 to 132V AC) 200- 240V AC +10% –15% (170 to 264V AC)
Input frequency		50/60Hz ± 5%	50/60Hz ± 5%	–	50/60Hz ± 5%	50/60Hz ± 5%
Max. input apparent power		110VA	110VA	65W	110VA	95VA
Inrush current		20A, within 8ms	20A, within 8ms	100A, within 1ms	20A, within 8ms	20A, within 8ms
Rated output current	5V DC	8A	5A	8A	2A	
	24V DC		0.8A		1.5A	1.2A
Overcurrent protection	5V DC	8.8A or higher	5.5A or higher	8.5A or higher	2.2A or higher	
	24V DC		1.2A or higher		2.3A or higher	1.7A or higher
Overvoltage protection	5V DC	5.5 to 6.5V	5.5 to 6.5V	5.5 to 6.9V	5.5 to 6.5V	
	24V DC		–		–	–
Efficiency		65% or higher	65% or higher	65% or higher	65% or higher	65% or higher
Power indicator		Power LED display	Power LED display	Power LED display	Power LED display	Power LED display
Terminal screw size		M4 x 0.7 x 6 (metric thread)				M3 x 0.5 x 6 (metric thread)
Wire size		0.75 to 2mm² (18–14AWG)				
Solderless terminal		To fit 4mm (0.157 inches)ϕ V1.25–4, V1.25–YS4A, V2–S4, V2- YS4A				To fit 3 mm (0.118 inches) ϕ V1.25–3, V1.25 YS3A, V2–S3, V2–YS3A
Tightening torque		17kg·cm (14.72lb·inches)				7kg·cm (6.06lb·inches)
External dimensions: mm (inches)		250 (9.84) x 37.5 (2.17) x 121 (4.76)				250 (9.84) x 37.5 (1.48) x 121 (4.76)
Weight kg (lb)		0.98 (2.16)	0.94 (2.07)	0.8 (1.76)	0.94 (2.07)	0.75 (1.65)

Table 3.9 Power Supply Unit Specifications

POINT

The A65P power supply unit (shaded) does not have sufficient power capacity for use in the same base unit as an A3HCPU.

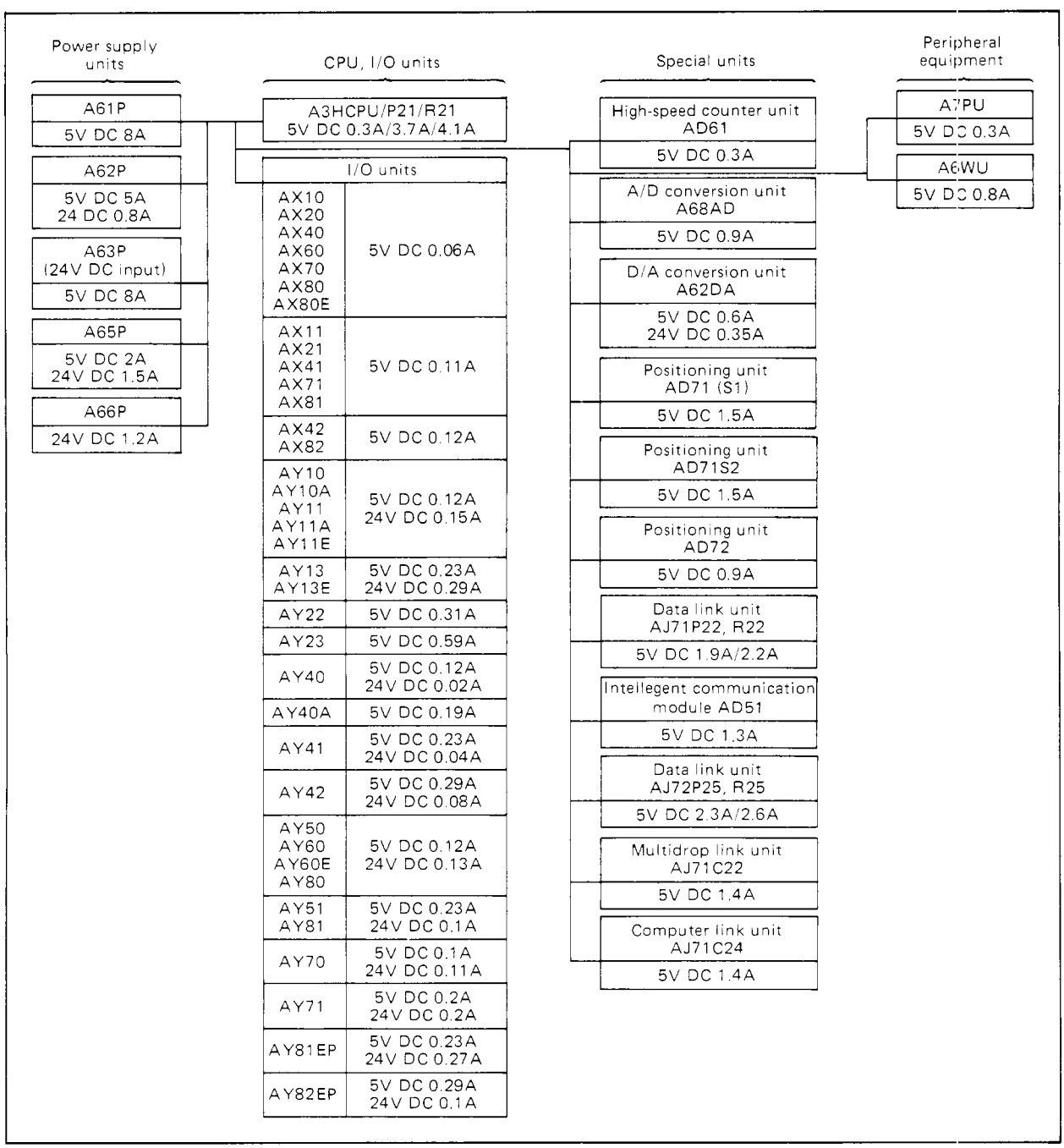
*** Note that the 5V capacity of the A62P power supply is limited. Care should be taken if using this unit in the same base unit as the A3HCPU.**

3.3.2 Power supply selection

Select the power supply unit according to the total 5V current consumption of all the I/O units, special units, and peripheral equipment supplied from that power supply. Note that the A55B and A58B extension bases draw their power requirements from the main base power supply.

(1) Current consumption of each unit

The current capacity of each power supply unit and the current consumption of each unit are indicated below. When a module does not appear on this table, consult the relevant module user's manual.



(2) Selection of power supply unit when extension base unit A55B or A58B is used.

The A55B and A58B extension base units receive their 5V DC supply from the main base unit via the extension cable.
When using either of these units, note the following:

(a) The 5V DC capacity of the main base unit power supply must be sufficient to cover the current consumption of both the main and the A55B/A58B extension base(s).

Example:
Assume that the 5V DC current consumption of the main base unit is 5A and of the A55B is 2A, the A61P (5V DC, 8A) must therefore be selected as the main base unit power supply.

(b) The power is supplied to the A55B or A58B via the extension cable, over which a voltage drop occurs. The voltage at the receiving end of the extension cable should not be lower than 4.75V DC.
For further information, refer to Section 3.4.3.

(3) Notes on use of the A66P

(a) The A66P gives optimum power output when a vacant slot exists on either side of it. It must be located without an I/O unit to the right, preferably with a vacant slot to the left.

(b) The A66P output current (24V DC) depends on the lefthand adjacent unit.

Left hand adjacent unit	Power Supply Unit	Input Unit Dummy Unit	Output Unit Special Function Unit	Vacant
Configuration	Power supply unit / A66P / Vacant	Input unit / Dummy unit / A66P / Vacant	Output unit / Special function unit / A66P / Vacant	Vacant / A66P / Vacant
Max. output current for 24V DC	0.5A	1.2A	1.0A	1.5A

Note: The vacant slot on the right hand end of the system is compulsory (alternatively, locate the A66P in the final I/O slot of the base)

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3.4 Base Unit Specifications

3.4.1 Main base unit specifications

Item \ Type	A32B	A35B	A38B
I/O unit capacity	2 units	5 units	8 units
Extension connection	No	Yes	Yes
Installation hole size	6mm (0.24 inches) dia. per-shaped hole (for M5 screw)		
External dimensions mm (inches)	247 (9.72) x 250 (9.84) x 29 (1.14)	382 (15.04) x 250 (9.84) x 29 (1.14)	480 (18.90) x 250 (9.84) x 29 (1.14)
Weight kg (lb)	0.96 (2.11)	1.5 (3.3)	1.9 (4.18)

(inches)

Table 3.10 Basic Base Unit Specifications

3.4.2 Extension base unit specifications

Item \ Type	A65B	A68B	A55B	A58B
I/O unit capacity	5 units	8 units	5 units	8 units
Power supply requirement	Power supply unit required		Power supply unit not required	
Installation hole size	6mm(0.24 inches) dia. pear-shaped hole (for M5 screw)		6mm (0.24 inches) dia. per-shaped hole (for M5 screw)	
Terminal screw size	–	–	M4 x 0.7 x 6 (FG termianl) (metric thread)	
Applicable wire size	–	–	1162.53 to 3100.09 in²	
Applicable solderless terminal size	–	–	To fit 4 mm (0.157 inches) ϕ (V)1.25-4, (V)1.25-YS4, (V)2-S4, (V)2-YS4A (Applicable tightening torque: 17kg·cm (14.72 lb·inches))	
External dimensions mm (inches)	352 (13.86) x 250 (9.84) x 29 (1.14)	446 (17.56) x 250 (9.84) x 29 (1.14)	297 (11.69) x 250 (9.84) x 29 (1.14)	411 (16.18) x 250 (9.84) x 29 (1.14)
Weight kg (lb)	1.4 (3.08)	1.9 (4.18)	1.2 (2.64)	1.7 (3.74)
Accessory	–		One dustproof cover (for I/O unit)	

Table 3.11 Extension Base Unit Specifications

POINT

When using either the A55B or A58B base unit refer to Section 3.3.2 "Selection of power supply unit" and Section 3.4.3.

3.4.3 Notes on the use of the A55B and A58B extension bases.

As discussed in section 3.3.2, a voltage drop occurs over the extension cable which is supplying the 5V DC from the main base to the A55B/A58B extension base.
Calculate the voltage drop as follows.

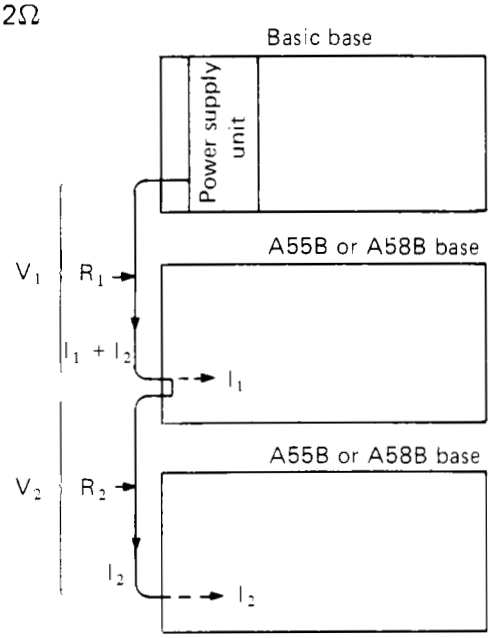
(1) Conditions

(a) The 5V DC output voltage from the power supply unit fluctuates by approx 0.1V. Hence in the worst case the supply voltage will drop to 4.9V.
(b) At least 4.75V DC should be available at the furthest base from the main base unit.

(2) Calculation of voltage at farthest unit.

Resistance of cable

AC06B 0.019Ω
AC12B 0.028Ω
AC30B 0.052Ω



V_1 : Voltage drop over cable between main base and extension base
V_2 : Voltage drop over cable between extension bases
R_1 : Resistance of cable between main base and extension base
R_2 : Resistance of cable between extension bases
I_1 : Current consumption (5V DC) of 1st extension stage
I_2 : Current consumption (5V DC) of 2nd extension stage

Voltage drops V_1 and V_2 are:

$V_1 = R_1 (I_1 + I_2)$
$V_2 = R_2 I_2$

The voltage at the receiving end of the 2nd extension stage must satisfy the following expression:

Farthest base voltage = $4.9 - (V_1 + V_2) > 4.75$

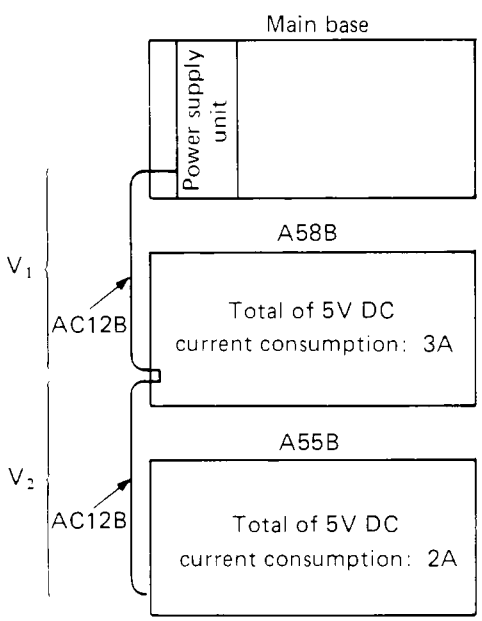
In order to satisfy the condition that the voltage at the final stage should be 4.75V or more, the following conditions should hold:

$$4.9 - 4.75 \geqq V_1 + V_2$$
$$0.15 \geqq R_1 (I_1 + I_2) + R_2 I_2$$

The above expressions are for two extension bases, where more than two are required:

Total voltage dropped over all the extension cables $\leqq$ 0.15V

(3) Calculation example



Resistance of AC12B = 0.028Ω
V_1 = 0.028 x (3 + 2) = 0.14 [V]
V_2 = 0.028 x 2 = 0.056 [V]

$V_1 + V_2$ = 0.196 [V]

(Receiving end voltage at 2nd extension stage is 4.9 − 0.196 = 4.704V)

The voltage drop is more than 0.15V, so that the 2nd extension base cannot be used.
If the two extension cables are replaced with (shorter length) AC06Bs.

V_1 = 0.019 x (3 + 2) = 0.095 [V]
V_2 = 0.019 x 2 = 0.038 [V]
$V_1 + V_2$ = 0.133 [V]

(Receiving end voltage at 2nd extension stage 4.9 − 0.133 = 4.767V)

The voltage drop is less than 0.15 so the system configuration is workable.

POINT

When using high current consumption I/O and special function units, use the A65B or A68B extension base with appropriate power supply.

3.5 Extension Cable Specifications

Item \ Type	AC06B	AC12B	AC30B
Cable length m (inch)	0.6 (23.62)	1.2 (47.24)	3 (118.11)
Resistance value of 5V DC supply line (Ω at 55°C)	0.019	0.028	0.052
Application	For connection between main and extension, and between extension bases		
Weight kg (lb)	0.34 (0.75)	0.53 (1.14)	1.06 (2.33)

Table 3.13 Extension Cable Specifications

3.6 Memory Specifications

3.6.1 Memory cassette specifications

Item \ Type	A3MCA-0	A3MCA-2	A3MCA-4	A3MCA-8	A3MCA-12	A3MCA-18
*Memory capacity (RAM capacity)	None installed	16K bytes	32K bytes	64K bytes	96K bytes	144K bytes
Number of ROM loading sockets	2 pcs. (for 28 pins)					
Usable ROM	4KROM, 8KROM, 16KROM					
Usable RAM	4KRAM	None required (already installed)				
External dimensions mm (inches)	110 (4.33) x 79.5 (3.13) x 33 (1.30)					
Weight kg (lb)	0.12 (0.26)	0.13 (0.29)	0.14 (0.31)	0.15 (0.33)	0.16 (0.35)	0.17 (0.37)

*: Built in RAM capacity.

Table 3.14 Memory Cassette Specifications

3.6.2 IC memory specifications

Item \ Type	4KRAM	4KROM	8KROM	16KROM
Memory specifications	IC-RAM	EP-ROM		
Memory capacity	8K bytes	8K bytes	16K bytes	32K bytes
Structure	28-pin IC package	28-pin IC package	28-pin IC package	28-pin IC package
Remarks	Two identical memory i.c.s are required per program.			

Table 3.15 Memory Specifications

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3.7 Fuse Specifications

Item \ Type	GTH4	MF51NM8	HP-32	HP-70K	MP-20	MP-32	MP-50
Application	For power supply unit A61P, A62P, A65P, A66P	For output unit AY11E, AY13E	For output unit AY23	For output unit AY22	For output unit AY50, AY80	For output unit AY60	For output unit AY60E
Shape	Cartridge type	Cartridge type	Plug type	Plug type	Plug type	Plug type	Plug type
Rated current	4A	8A	3.2A	7A	2A	3.2A	5A
External dimensions mm (inches)	φ6 (0.24) x 32 (1.26)	φ5.2 (0.20) x 20 (0.79)	30.3 (1.19) x 8 (0.31) x 20 (0.79)	30.3 (1.19) x 8 (0.31) x 20 (0.79)	17.2 (0.68) x 5.5 (0.22) x 19 (0.75)	17.2 (0.68) x 5.5 (0.22) x 19 (0.75)	17.2 (0.68) x 5.5 (0.22) x 19 (0.75)

Table 3.16 Fuse Specifications

3.8 Battery Specifications

This section gives the specifications of the battery used for RAM memory backup and power failure compensation.

Item \ Type	A6BAT
Nominal voltage	3.6V DC
Guaranteed life	5 years
Total power failure backup time	Depends on memory cassette types as indicated below: A3MCA-0: Min. 10800 hours, A3MCA-18: Min. 1950 hours
Application	For IC-RAM memory backup and power failure compensation function
External dimensions mm (inches)	φ16 (0.63) x 30 (1.18)

Table 3.17 Battery Specifications

4. HANDLING

This section gives handling instructions, PC nomenclature and hardware setting instructions.

4.1 Handling Instructions

4.1.1 Main unit

(1) Do not subject the unit to impact loads.

(2) Do not remove printed circuit boards from the housing. There are no user-serviceable parts on the boards.

(3) Ensure that no conductive debris can enter the unit, if it does, make sure that it is removed. Guard particularly against wire offcuts.

(4) Tighten unit mounting and terminal screws, as specified below.

Screw	Tightening Torque Range kg·cm (lb·inches)
I/O unit terminal screws	5 (4.33) to 8 (6.93)
I/O unit terminal block installation screws	8 (6.93) to 14 (12.13)
Power supply unit terminal screws	10 (8.66) to 14 (12.13)
Unit mounting screws (optional)	8 (6.93) to 12 (10.39)

4.1.2 Memory (Memory cassete)

(1) When loading the memory cassette into the main unit, press the memory cassette securely into the housing.

(2) When loading the IC memory into the socket, press the i.c. securely against the socket and then lock it. After loading. check that the i.c. is flush with the socket.

(3) Do not place an IC memory on a conductive or charged surface. (e.g. wood, plastic, vinyl, fibre, cable, paper)

(4) Do not touch or bend the IC memory pins.

(5) Ensure that IC memories are installed the right way round in the memory socket (as illustrated on the socket). Wrongly installed i.c. memories will be damaged.

(6) Do not touch the CPU memory cassette connector.

IMPORTANT

Switch off the power before installing or removing the memory cassette to or from the CPU or GPP. Installing or removing the memory cassette with the power on can lead to memory corruption.

4.1.3 Battery

(1) Do not short-circuit.

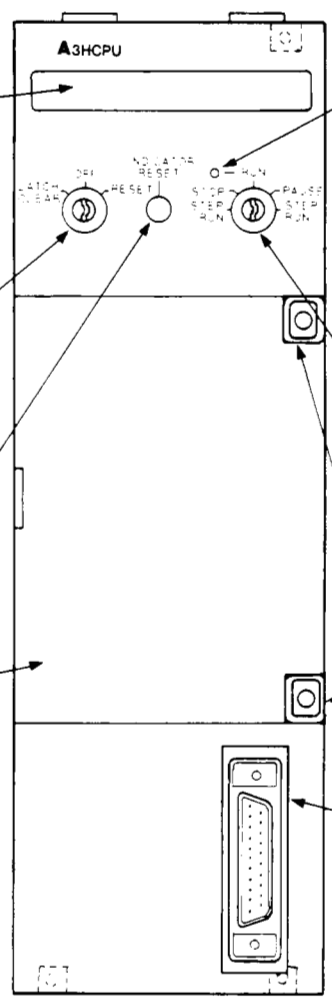
(2) Do not disassemble.

(3) Do not burn.

(4) Do not heat. (max. 75°C)

(5) Do not solder the battery terminals.

4.2 Nomenclature



LED display

Displays up to 16 alphanumeric characters. May be addressed from the user program using the LED commands and/or displays self diagnosed error messages.

Reset key switch

RESET: Hardware reset
Used to reset the CPU after an operation error and to initialize operation. The latch memory is not cleared when the CPU is reset.
LATCH CLEAR:
Sets all latch area data (as defined in parameters) to OFF or "0".
(Valid when the CPU is in STOP status)

LED display reset switch

Clears the present LED annunciator message. The Next message in the annunciator queue is then displayed where appropriate.

Memory cassette

- Memory locations for sequence, subsequence programs, comments, file registers etc.
- Has built-in memory protect switches.

RUN LED

Indicates the run status of the CPU.

On:	The CPU is in RUN or STEP RUN status, no operation errors have occured, the program is being run and the PC is active.
Off:	The CPU is in STOP, PAUSE or STEP RUN status and the program is not being run.
Flicker:	Self diagnosed error has occurred.

RUN/STOP key switch

RUN:	To run the PC program.
STOP:	To terminate running the PC program.
PAUSE:	To terminate running the PC program and maintain output status.
STEP RUN:	To run the program step by step/scan by scan.

Memory cassette release latch

Press the two latches to remove the memory cassette.

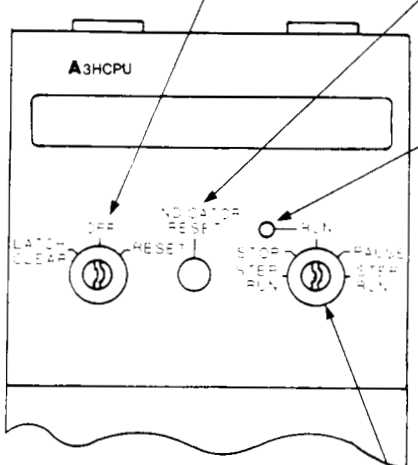
RS422 connector

Peripheral programmer port. Fit cover (supplied) when not in use.

REMARKS

The shaded items require setting up before using the unit.

Details of switches and indicators



- "LATCH CLEAR-RESET" . . . . . Reset key switch
  LATCH CLEAR: Sets all latch area data (as defined in parameters) to OFF or "0".

  RESET: Used to reset the CPU after an operation error and to initialize operation.
  Any errors which have occurred during operation should be reset with this switch and corrected.
  All data outside the latch area is cleared when the CPU is reset

  OFF: The keyswitch is spring loaded to return to this position after the CPU has been reset or latch data cleared.

- "INDICATOR RESET" . . . . . Display reset switch
  Clears annunciator (F) number or its ASCII comment from the LED display.

- "RUN" . . . . . RUN indicator LED
  This LED indicates that the PC is running. When the RUN-STOP-PAUSE-STEP RUN select key switch is at the "RUN" position and program operation is being executed normally, the LED is lit. The RUN LED is also lit when the key switch is in the STEP RUN position and step run is being implemented and when the keyswitch is in the PAUSE position and pause status is not being implemented. (e.g. M9040 off)
  When the CPU is in STOP or PAUSE status the RUN LED is unlit.
  The RUN LED is also unlit when the keyswitch is in the STEP RUN position but step run is not being implemented or when an operation error causes the PC CPU to switch out of run status.

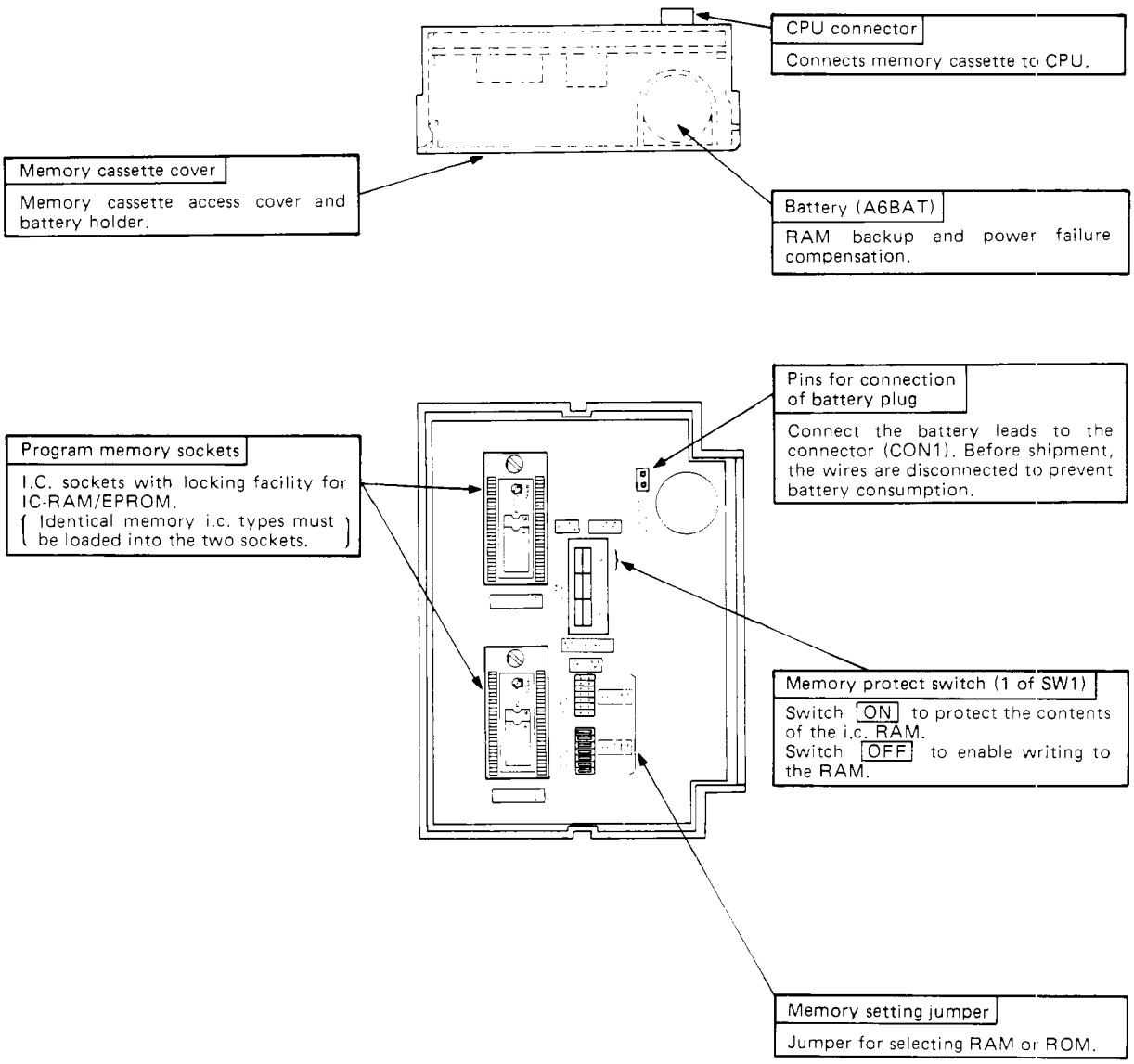
- "STEP RUN-STOP-RUN-PAUSE-STEP RUN" . . . . . Run/stop/pause/step run select switch
  This keyswitch enables "RUN", "STOP", "PAUSE", or "STEP RUN" status.

To run the PC program move this switch to the "RUN" position. When the power is switched on with the switch at the "RUN" position, operation is initiated immediatly.
To stop program processing, move the keyswitch from the "RUN" to "STOP" position. All output points are turned off. This is a temporary stop and all control information remains unchanged. Moving the switch back to the "RUN" position without resetting the CPU, resumes processing using the previous data.
The "PAUSE" function causes the PC to stop with the output state held. Use this function in conjuction with special relays M9040 and M9041.
"STEP RUN" is a fault finding facility which is initiated from the GPP/PHP/HGP. Step run may be processed in one of two ways:

Step run . . . . . .The program is run step by step.
Loop count specification . . . . . .The program is run scan by scan.

4.3 Memory Cassette Nomenclature

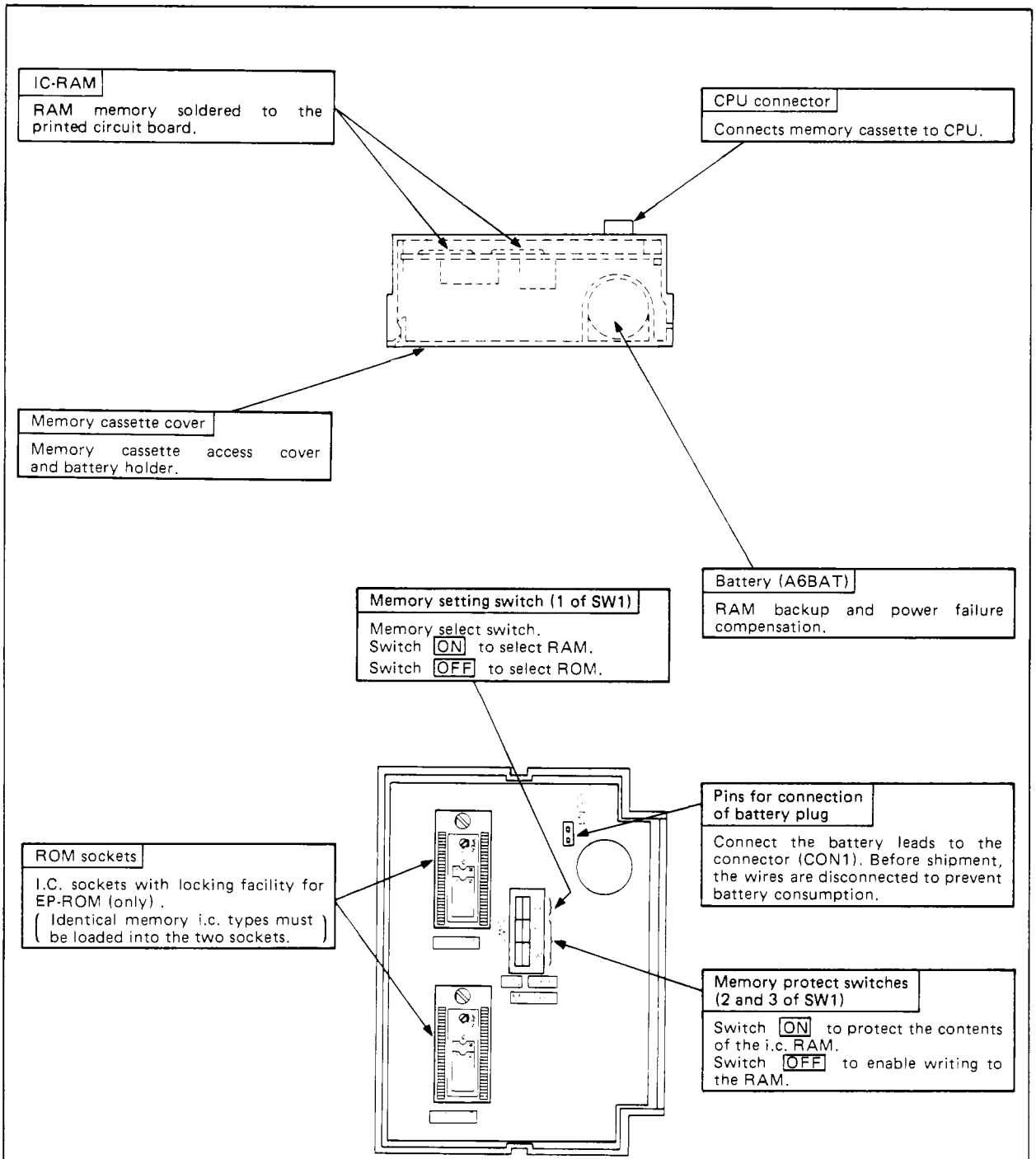
(1) A3MCA-0


CPU connector
Connects memory cassette to CPU.
Memory cassette cover
Memory cassette access cover and battery holder.
Battery (A6BAT)
RAM backup and power failure compensation.
Pins for connection of battery plug
Connect the battery leads to the connector (CON1). Before shipment, the wires are disconnected to prevent battery consumption.
Program memory sockets
I.C. sockets with locking facility for IC-RAM/EPROM.
(Identical memory i.c. types must be loaded into the two sockets.)
Memory protect switch (1 of SW1)
Switch ON to protect the contents of the i.c. RAM.
Switch OFF to enable writing to the RAM.
Memory setting jumper
Jumper for selecting RAM or ROM.

REMARKS

The shaded items require setting before using the unit.

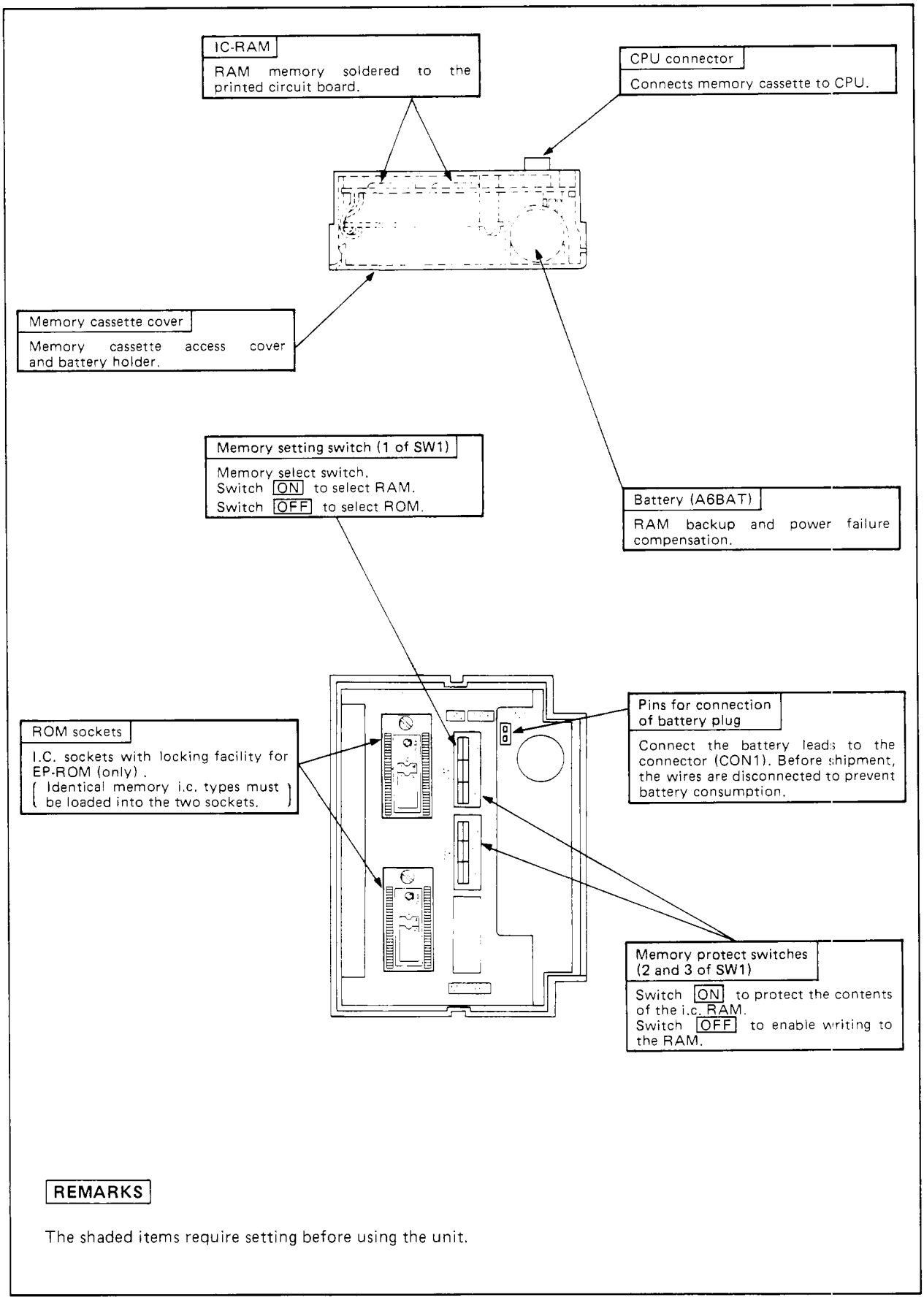
(2) A3MCA-2, A3MCA-4


IC-RAM
RAM memory soldered to the printed circuit board.
CPU connector
Connects memory cassette to CPU.
Memory cassette cover
Memory cassette access cover and battery holder.
Battery (A6BAT)
RAM backup and power failure compensation.
Memory setting switch (1 of SW1)
Memory select switch.
Switch ON to select RAM.
Switch OFF to select ROM.
Pins for connection of battery plug
Connect the battery leads to the connector (CON1). Before shipment, the wires are disconnected to prevent battery consumption.
ROM sockets
I.C. sockets with locking facility for EP-ROM (only).
(Identical memory i.c. types must be loaded into the two sockets.)
Memory protect switches (2 and 3 of SW1)
Switch ON to protect the contents of the i.c. RAM.
Switch OFF to enable writing to the RAM.

REMARKS

The shaded items require setting before using the unit.

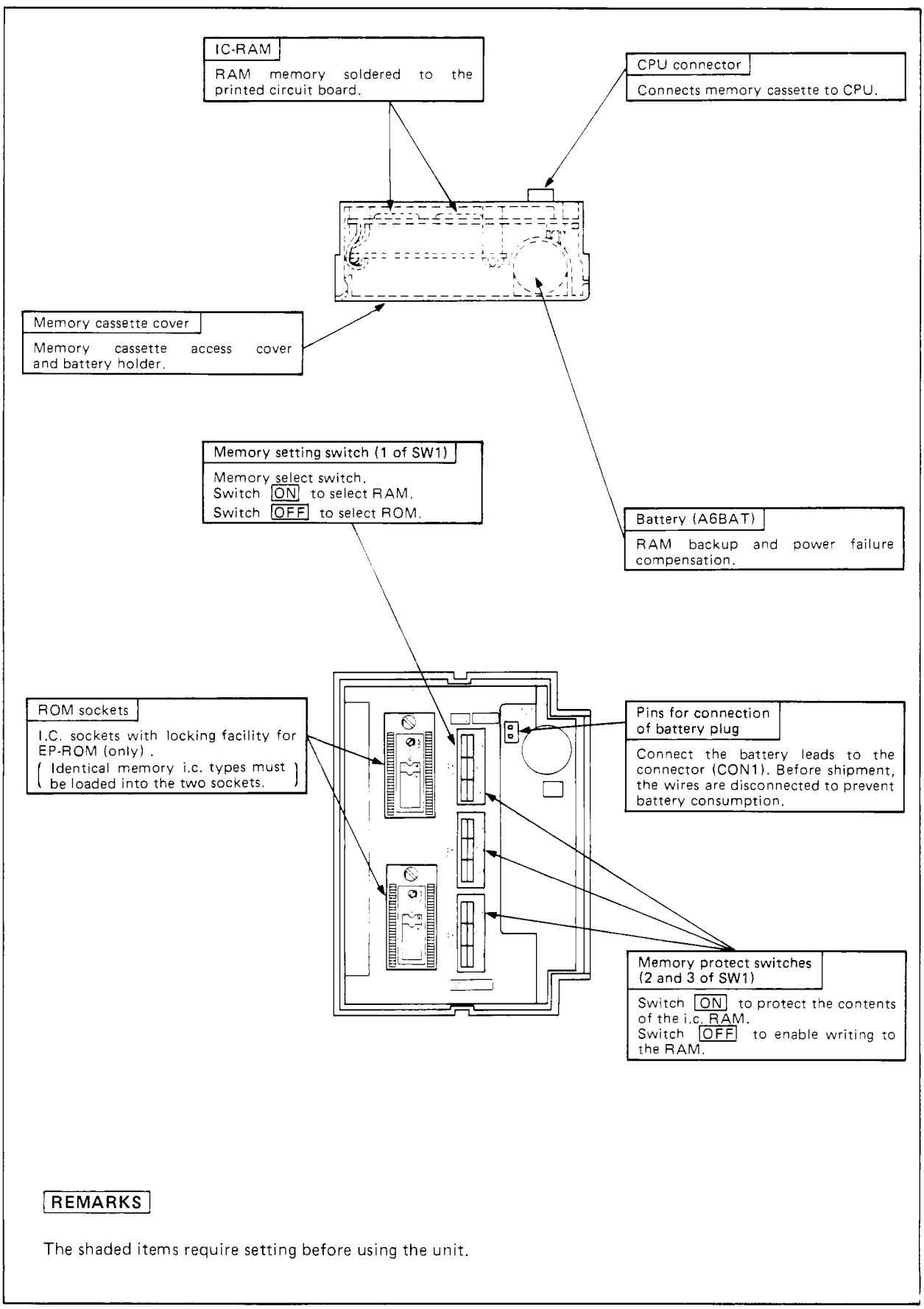
(3) A3MCA-8


IC-RAM
RAM memory soldered to the printed circuit board.
CPU connector
Connects memory cassette to CPU.
Memory cassette cover
Memory cassette access cover and battery holder.
Memory setting switch (1 of SW1)
Memory select switch.
Switch ON to select RAM.
Switch OFF to select ROM.
Battery (A6BAT)
RAM backup and power failure compensation.
ROM sockets
I.C. sockets with locking facility for EP-ROM (only).
(Identical memory i.c. types must be loaded into the two sockets.)
Pins for connection of battery plug
Connect the battery leads to the connector (CON1). Before shipment, the wires are disconnected to prevent battery consumption.
Memory protect switches (2 and 3 of SW1)
Switch ON to protect the contents of the i.c. RAM.
Switch OFF to enable writing to the RAM.

REMARKS

The shaded items require setting before using the unit.

(4) A3MCA-12, A3MCA-18


IC-RAM
RAM memory soldered to the printed circuit board.
CPU connector
Connects memory cassette to CPU.
Memory cassette cover
Memory cassette access cover and battery holder.
Memory setting switch (1 of SW1)
Memory select switch.
Switch ON to select RAM.
Switch OFF to select ROM.
Battery (A6BAT)
RAM backup and power failure compensation.
ROM sockets
I.C. sockets with locking facility for EP-ROM (only).
(Identical memory i.c. types must be loaded into the two sockets.)
Pins for connection of battery plug
Connect the battery leads to the connector (CON1). Before shipment, the wires are disconnected to prevent battery consumption.
Memory protect switches (2 and 3 of SW1)
Switch ON to protect the contents of the i.c. RAM.
Switch OFF to enable writing to the RAM.

REMARKS

The shaded items require setting before using the unit.

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4.4 Memory cassette preparation

Before operation, various switch settings must be made in the memory cassette as well as battery installation etc.

4.4.1 Memory i.c. installation

(1) A3MCA-0

RAM or ROM must be installed and switch settings made, as follows:

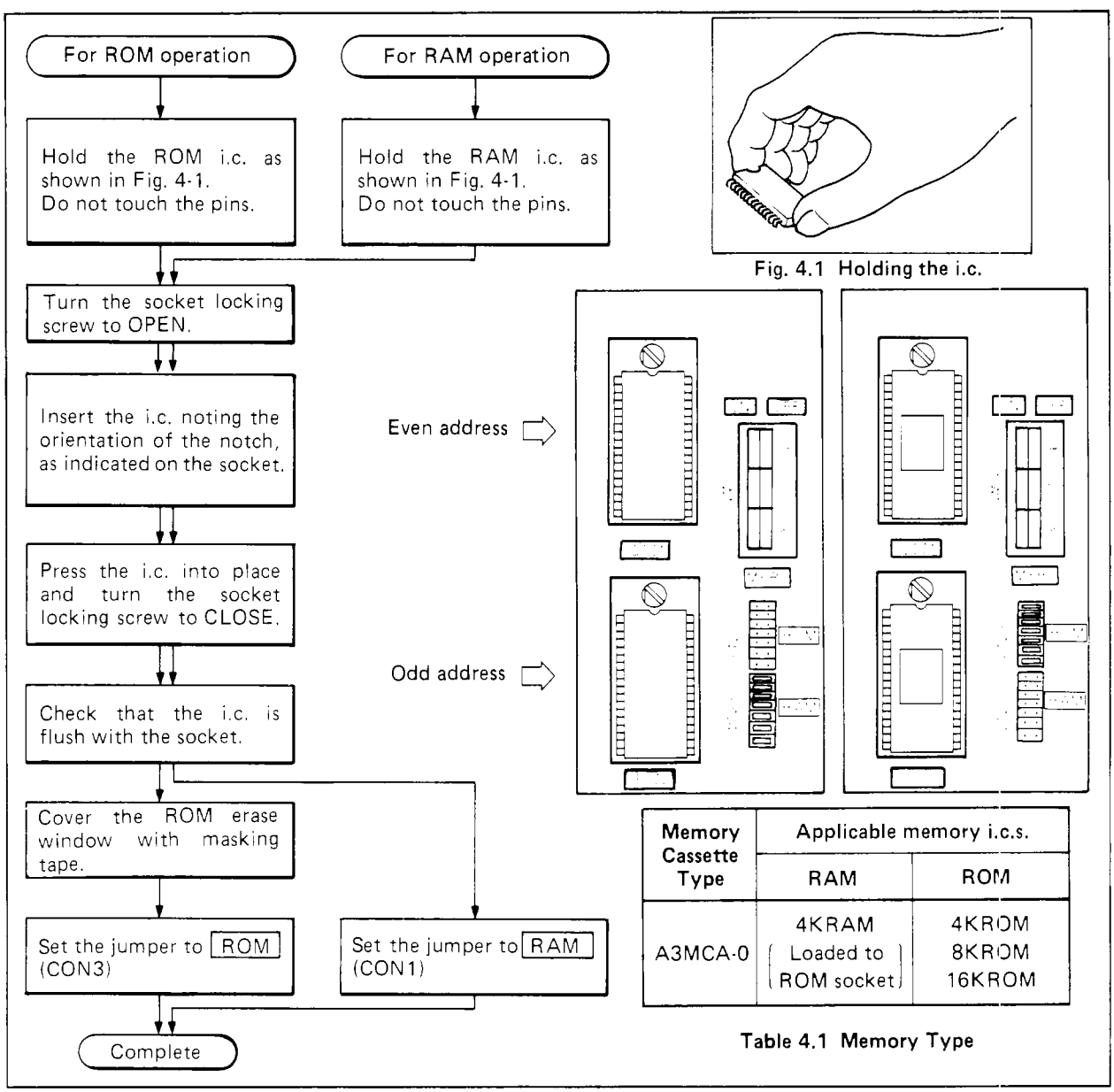

For ROM operation
For RAM operation
Hold the ROM i.c. as shown in Fig. 4-1. Do not touch the pins.
Hold the RAM i.c. as shown in Fig. 4-1. Do not touch the pins.
Turn the socket locking screw to OPEN.
Insert the i.c. noting the orientation of the notch, as indicated on the socket.
Press the i.c. into place and turn the socket locking screw to CLOSE.
Check that the i.c. is flush with the socket.
Cover the ROM erase window with masking tape.
Set the jumper to ROM (CON3)
Set the jumper to RAM (CON1)
Complete
Even address
Odd address

Fig. 4.1 Holding the i.c.

Memory Cassette Type	Applicable memory i.c.s.	
	RAM	ROM
A3MCA-0	4KRAM (Loaded to ROM socket)	4KROM 8KROM 16KROM

Table 4.1 Memory Type

POINT

The even address memory i.c. (in SOC1) and the odd address memory i.c. (in SOC2) must both be of the same type. The PC will not operate if memories are swapped.

(2) A3MCA-2 to A3MCA-18

ROM (optional) installation and switch settings are made as follows:

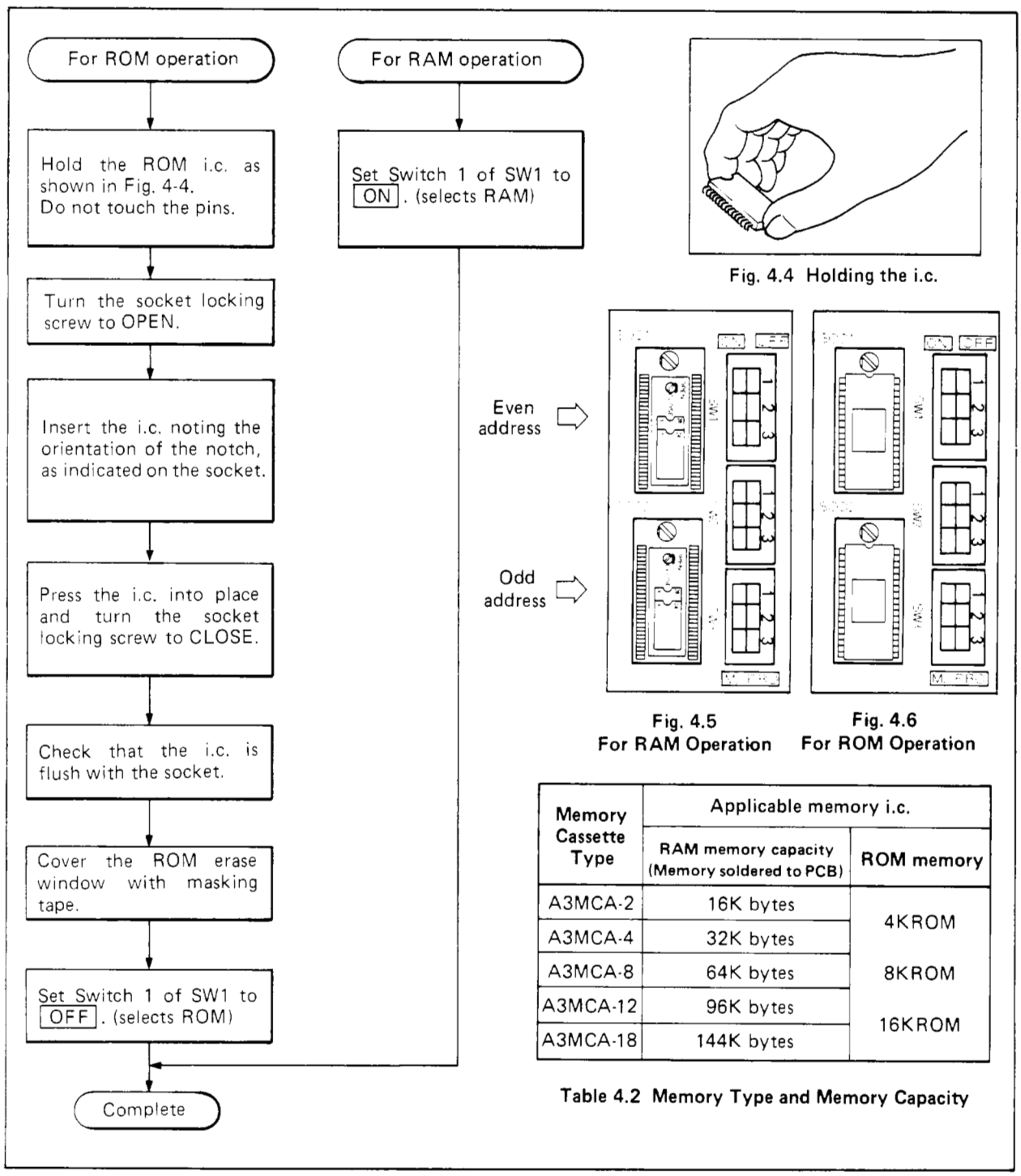

For ROM operation
For RAM operation
Hold the ROM i.c. as shown in Fig. 4-4. Do not touch the pins.
Set Switch 1 of SW1 to ON. (selects RAM)
Turn the socket locking screw to OPEN.
Insert the i.c. noting the orientation of the notch, as indicated on the socket.
Press the i.c. into place and turn the socket locking screw to CLOSE.
Check that the i.c. is flush with the socket.
Cover the ROM erase window with masking tape.
Set Switch 1 of SW1 to OFF. (selects ROM)
Complete
Even address
Odd address

Fig. 4.4 Holding the i.c.

Fig. 4.5
For RAM Operation

Fig. 4.6
For ROM Operation

Memory Cassette Type	Applicable memory i.c.	
	RAM memory capacity (Memory soldered to PCB)	ROM memory
A3MCA-2	16K bytes	4KROM
A3MCA-4	32K bytes	
A3MCA-8	64K bytes	8KROM
A3MCA-12	96K bytes	16KROM
A3MCA-18	144K bytes	

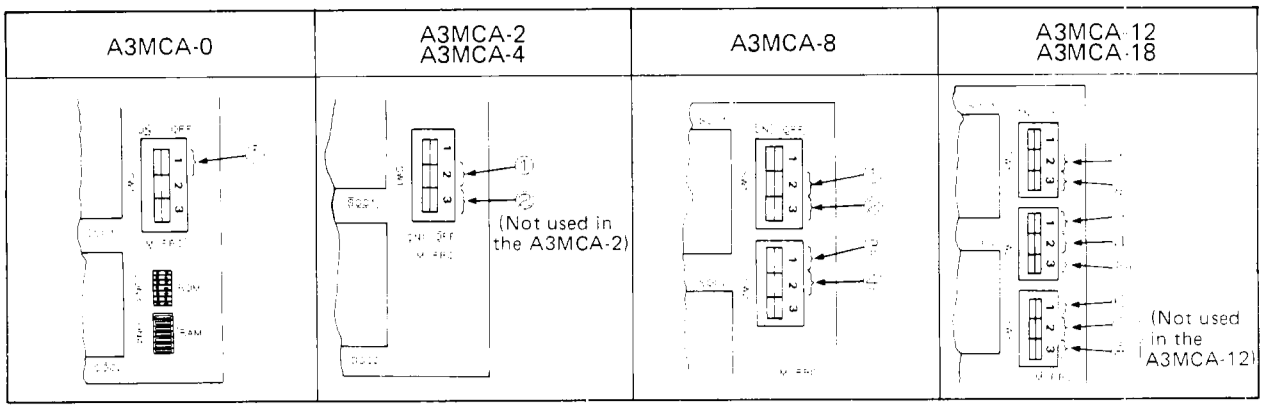
Table 4.2 Memory Type and Memory Capacity

POINT

The even address memory i.c. (in SOC1) and the odd address memory i.c. (in SOC2) must both be of the same type. The PC will not operate if memories are swapped.

4.4.2 Memory protect switch setting

The RAM memory may be protected by switching the memory protect switch ON. (See below)
This protects the memory from accidental program changes.
When changes to the PC program are to be made, switch the memory protect switch OFF.
The switch layout varies depending on the memory cassette type as shown below.



The memory ranges protected by each switch are shown below:

Step number	Byte number		
0 to 8191	0 to 16K	Memory protect range with switch 1 on	Applies to the A3MCA-0 and -2
8192 to 16383	16K to 32K	Memory protect range with switch 2 on	Applies to the A3MCA-4
16384 to 24575	32K to 48K	Memory protect range with switch 3 on	Applies to the A3MCA-8
24576 to 32767	48K to 64K	Memory protect range with switch 4 on	Applies to the A3MCA-12
32768 to 40959	64K to 80K	Memory protect range with switch 5 on	Applies to the A3MCA-18
40960 to 49151	80K to 96K	Memory protect range with switch 6 on	
49152 to 57343	96K to 112K	Memory protect range with switch 7 on	
57344 to 73727	112K to 144K	Memory protect range with switch 8 on	

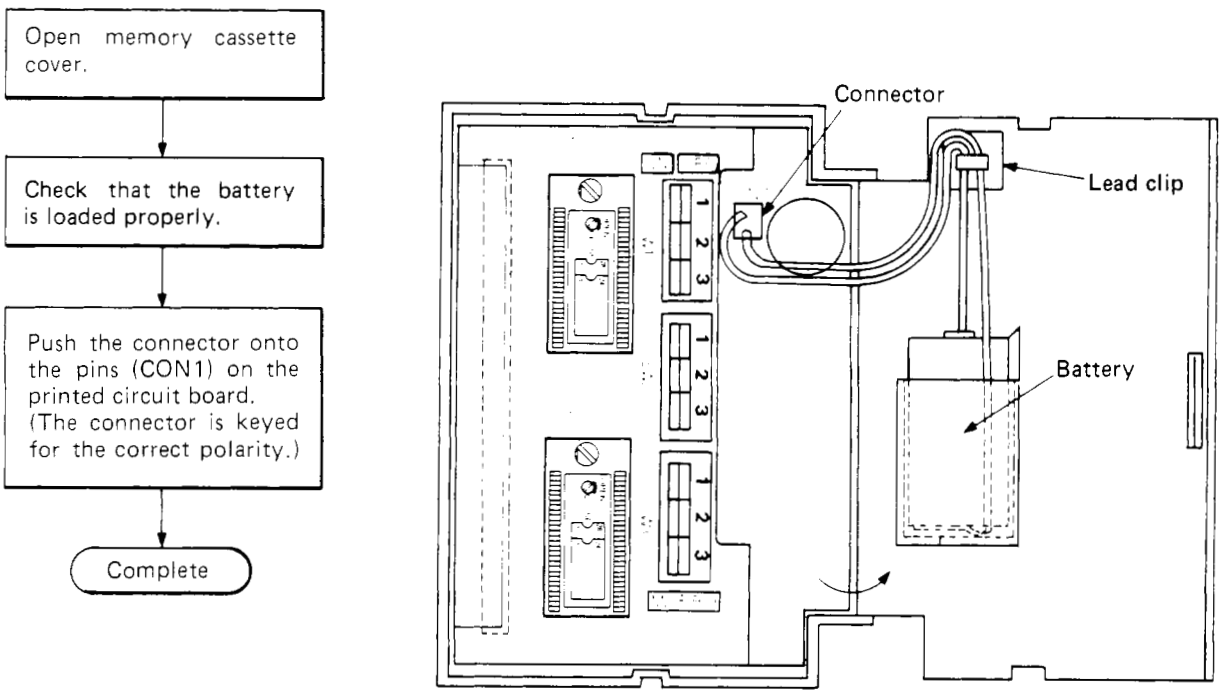
POINT

1. Select the memory areas to be protected after making any user memory parameter assignments (see Section 3.2.2) and ensure that only valid RAM areas are protected. Do not memory protect RAM work areas (e.g. for microcomputer programs) or file register areas.

2. Do not memory protect areas required for sampling trace or status latch data when using these functions.

4.4.3 Battery installation

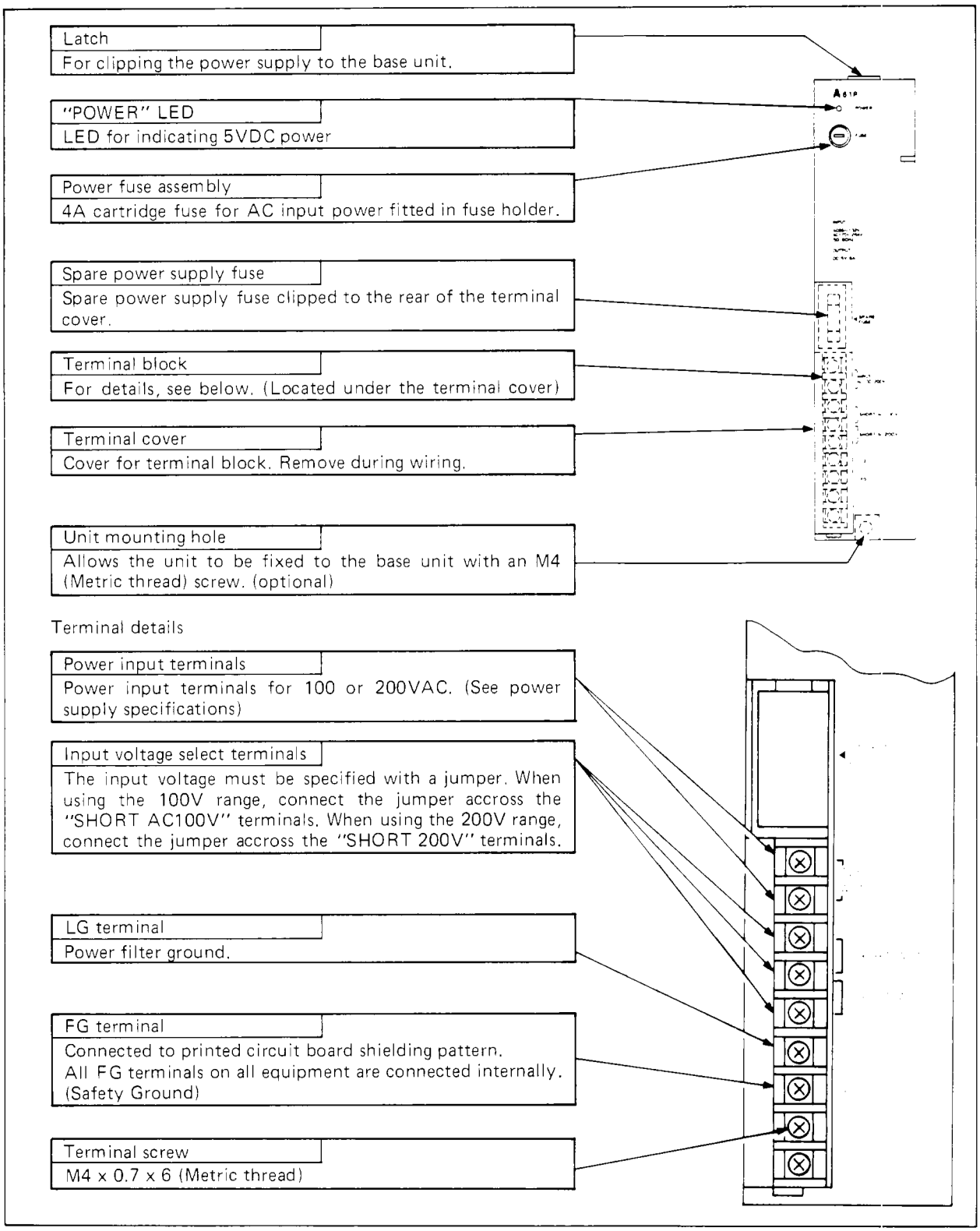
The battery connector has been disconnected before shipment. Where RAM backup and/or power failure memory retention is required connect the battery as shown below:


Open memory cassette cover.
Check that the battery is loaded properly.
Push the connector onto the pins (CON1) on the printed circuit board. (The connector is keyed for the correct polarity.)
Complete
Connector
Lead clip
Battery

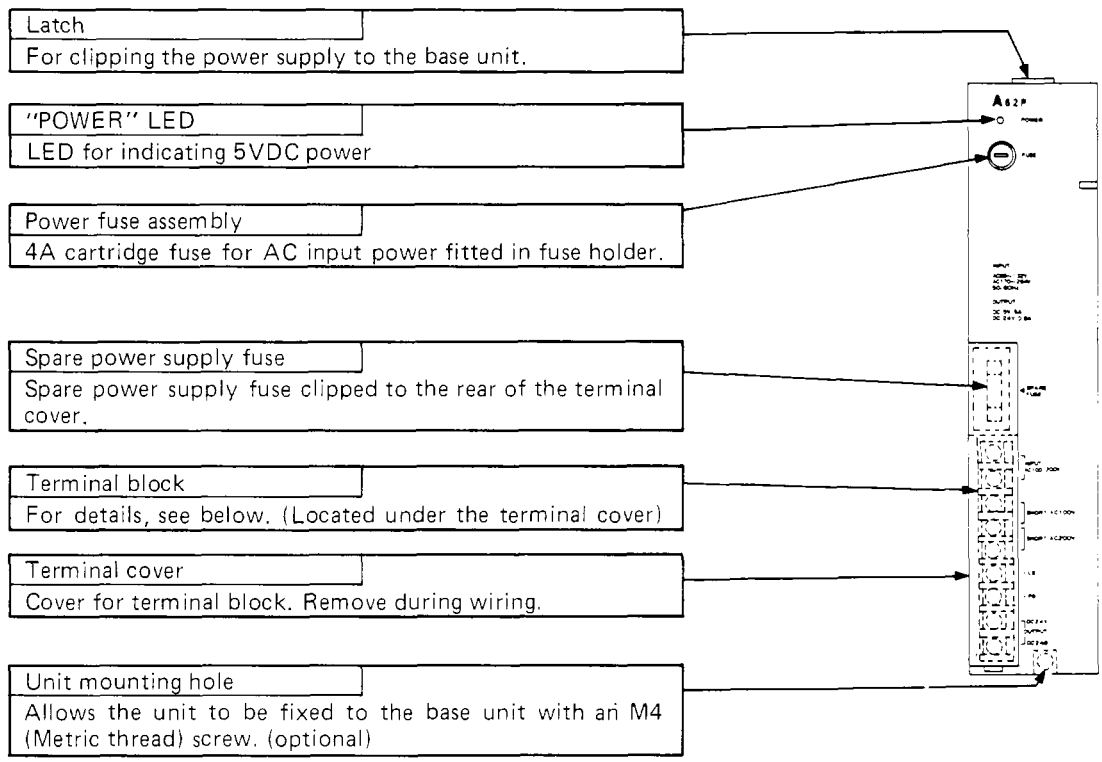
4.5 Power Supply Units

4.5.1 Nomenclature

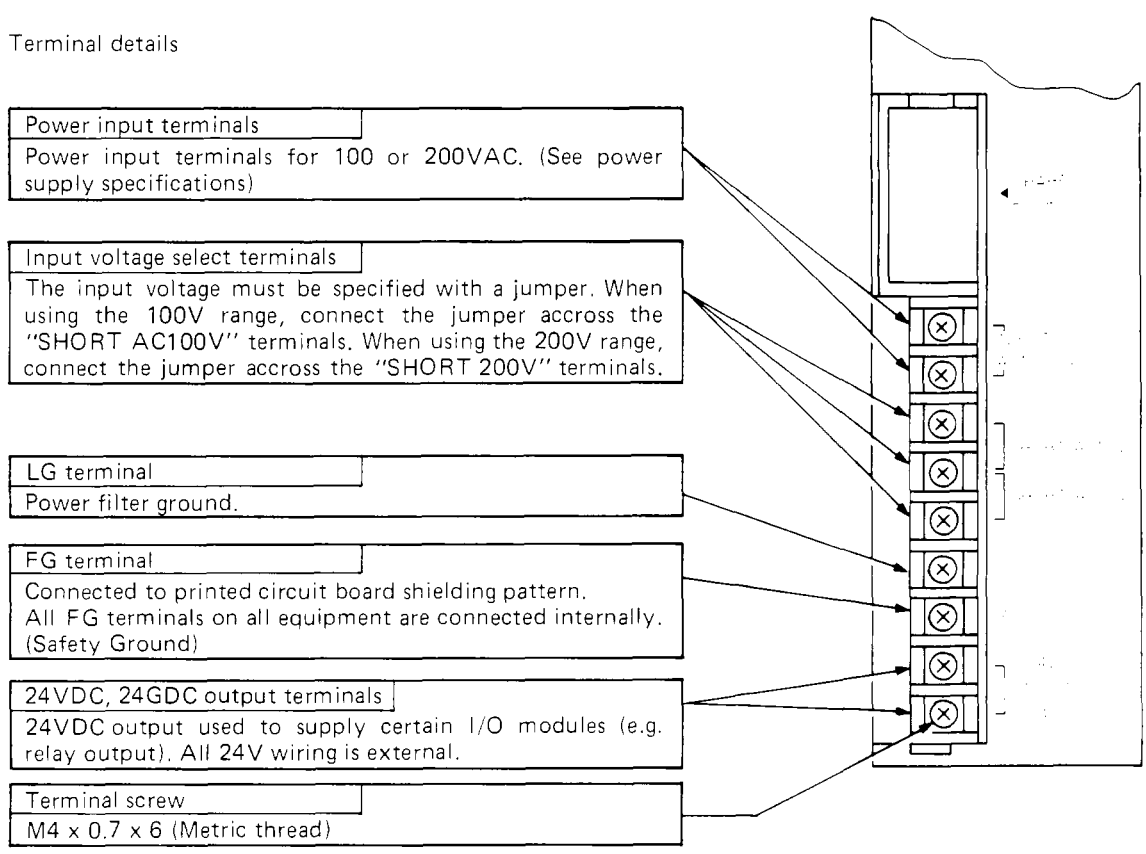
(1) A61P


Latch
For clipping the power supply to the base unit.
"POWER" LED
LED for indicating 5VDC power
Power fuse assembly
4A cartridge fuse for AC input power fitted in fuse holder.
Spare power supply fuse
Spare power supply fuse clipped to the rear of the terminal cover.
Terminal block
For details, see below. (Located under the terminal cover)
Terminal cover
Cover for terminal block. Remove during wiring.
Unit mounting hole
Allows the unit to be fixed to the base unit with an M4 (Metric thread) screw. (optional)
Terminal details
Power input terminals
Power input terminals for 100 or 200VAC. (See power supply specifications)
Input voltage select terminals
The input voltage must be specified with a jumper. When using the 100V range, connect the jumper accross the "SHORT AC100V" terminals. When using the 200V range, connect the jumper accross the "SHORT 200V" terminals.
LG terminal
Power filter ground.
FG terminal
Connected to printed circuit board shielding pattern.
All FG terminals on all equipment are connected internally.
(Safety Ground)
Terminal screw
M4 x 0.7 x 6 (Metric thread)

(2) A62P, A65P


Latch
For clipping the power supply to the base unit.
"POWER" LED
LED for indicating 5VDC power
Power fuse assembly
4A cartridge fuse for AC input power fitted in fuse holder.
Spare power supply fuse
Spare power supply fuse clipped to the rear of the terminal cover.
Terminal block
For details, see below. (Located under the terminal cover)
Terminal cover
Cover for terminal block. Remove during wiring.
Unit mounting hole
Allows the unit to be fixed to the base unit with an M4 (Metric thread) screw. (optional)

Terminal details


Power input terminals
Power input terminals for 100 or 200VAC. (See power supply specifications)
Input voltage select terminals
The input voltage must be specified with a jumper. When using the 100V range, connect the jumper accross the "SHORT AC100V" terminals. When using the 200V range, connect the jumper accross the "SHORT 200V" terminals.
LG terminal
Power filter ground.
FG terminal
Connected to printed circuit board shielding pattern.
All FG terminals on all equipment are connected internally.
(Safety Ground)
24VDC, 24GDC output terminals
24VDC output used to supply certain I/O modules (e.g. relay output). All 24V wiring is external.
Terminal screw
M4 x 0.7 x 6 (Metric thread)

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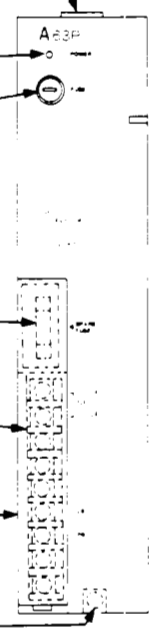
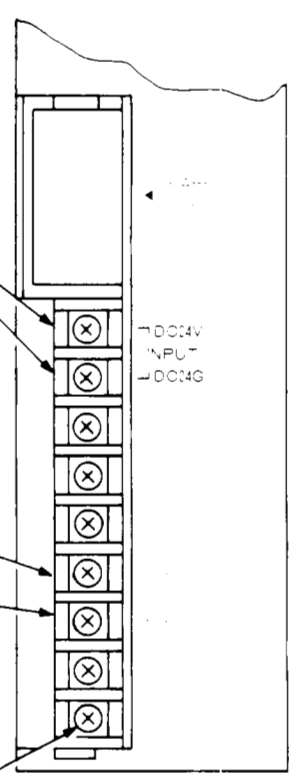
(3) A63P

Latch	For clipping the power supply to the base unit.
"POWER" LED	LED for indicating 5VDC power
Power fuse assembly	4A cartridge fuse for AC input power fitted in fuse holder.
Spare power supply fuse	Spare power supply fuse clipped to the rear of the terminal cover.
Terminal block	For details, see below. (Located under the terminal cover)
Terminal cover	Cover for terminal block. Remove during wiring.
Unit mounting hole	Allows the unit to be fixed to the base unit with an M4 (Metric thread) screw. (optional)

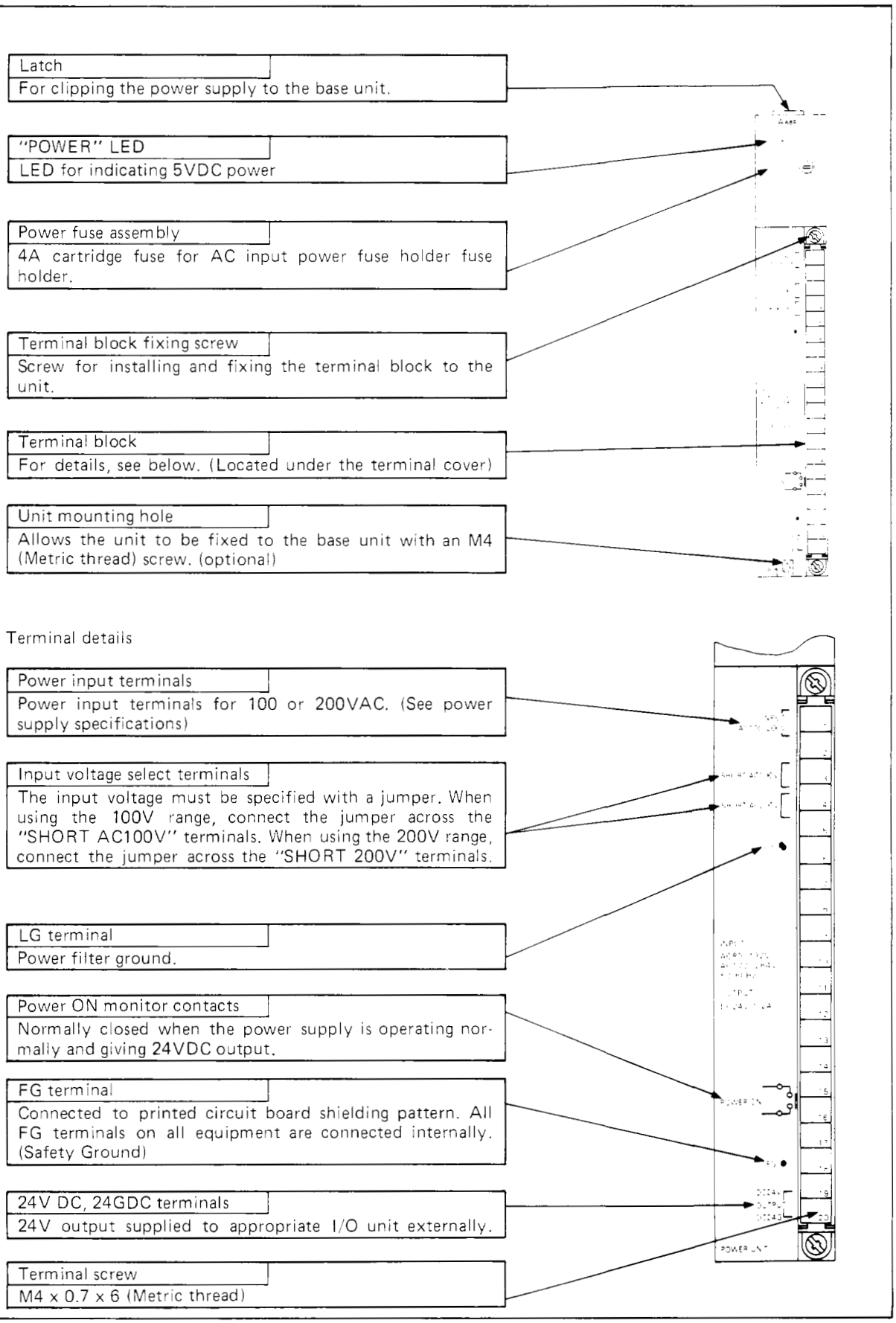


Terminal details

Power input terminals	Power input terminals for 24V DC.
LG terminal	Power filter ground.
FG terminal	Connected to printed circuit board shielding pattern. All FG terminals on all equipment are connected internally. (Safety Ground)
Terminal screw	M4 x 0.7 x 6 (Metric thread)

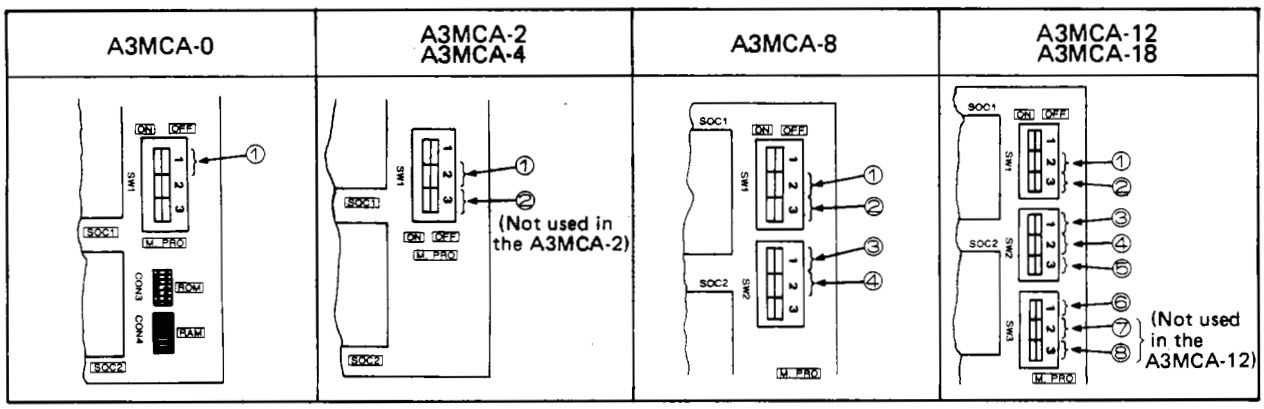


(4) A66P


Latch
For clipping the power supply to the base unit.
"POWER" LED
LED for indicating 5VDC power
Power fuse assembly
4A cartridge fuse for AC input power fuse holder fuse holder.
Terminal block fixing screw
Screw for installing and fixing the terminal block to the unit.
Terminal block
For details, see below. (Located under the terminal cover)
Unit mounting hole
Allows the unit to be fixed to the base unit with an M4 (Metric thread) screw. (optional)
Terminal details
Power input terminals
Power input terminals for 100 or 200VAC. (See power supply specifications)
Input voltage select terminals
The input voltage must be specified with a jumper. When using the 100V range, connect the jumper across the "SHORT AC100V" terminals. When using the 200V range, connect the jumper across the "SHORT 200V" terminals.
LG terminal
Power filter ground.
Power ON monitor contacts
Normally closed when the power supply is operating normally and giving 24VDC output.
FG terminal
Connected to printed circuit board shielding pattern. All FG terminals on all equipment are connected internally. (Safety Ground)
24V DC, 24GDC terminals
24V output supplied to appropriate I/O unit externally.
Terminal screw
M4 x 0.7 x 6 (Metric thread)

4.4.2 Memory protect switch setting

The RAM memory may be protected by switching the memory protect switch ON. (See below)
This protects the memory from accidental program changes.
When changes to the PC program are to be made, switch the memory protect switch OFF.
The switch layout varies depending on the memory cassette type as shown below.



The memory ranges protected by each switch are shown below:

Step number	Byte number		
0 to 8191	0 to 16K	Memory protect range with switch 1 on	Applies to the A3MCA-0 and -2
8192 to 16383	16K to 32K	Memory protect range with switch 2 on	Applies to the A3MCA-4
16384 to 24575	32K to 48K	Memory protect range with switch 3 on	Applies to the A3MCA-8
24576 to 32767	48K to 64K	Memory protect range with switch 4 on	Applies to the A3MCA-12
32768 to 40959	64K to 80K	Memory protect range with switch 5 on	Applies to the A3MCA-18
40960 to 49151	80K to 96K	Memory protect range with switch 6 on	
49152 to 57343	96K to 112K	Memory protect range with switch 7 on	
57344 to 73727	112K to 144K	Memory protect range with switch 8 on	

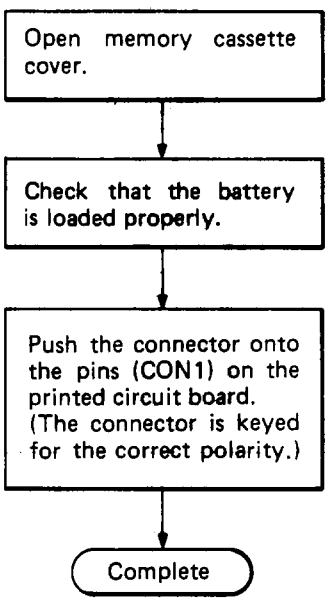
POINT

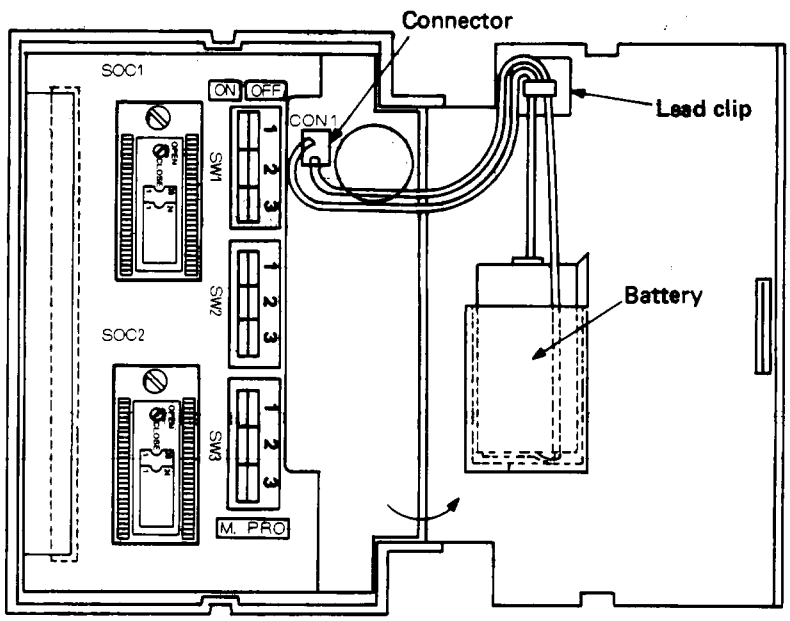
1. **Select the memory areas to be protected after making any user memory parameter assignments (see Section 3.2.2) and ensure that only valid RAM areas are protected. Do not memory protect RAM work areas (e.g. for microcomputer programs) or file register areas.**

2. **Do not memory protect areas required for sampling trace or status latch data when using these functions.**

4.4.3 Battery installation

The battery connector has been disconnected before shipment. Where RAM backup and/or power failure memory retention is required connect the battery as shown below:

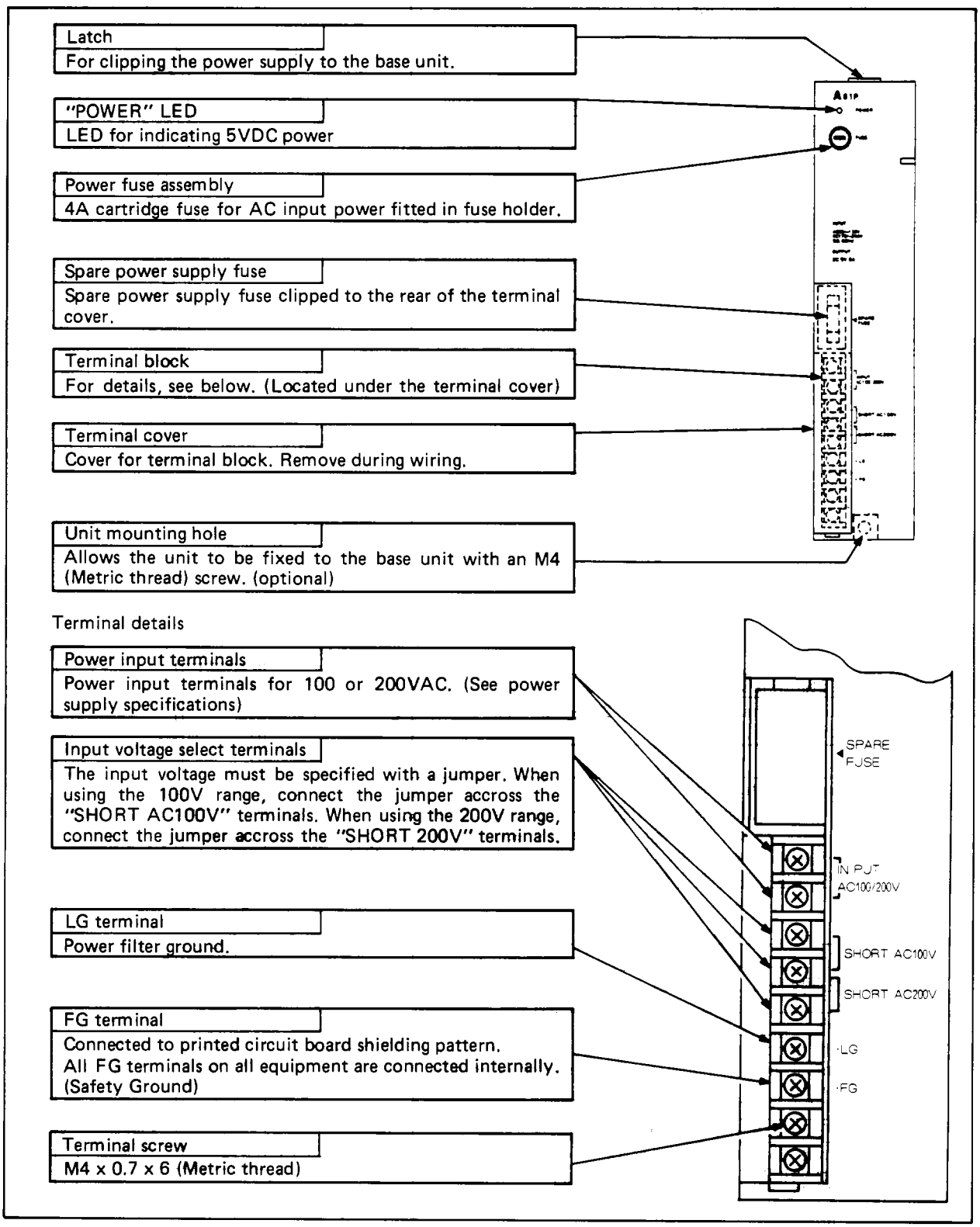

Open memory cassette cover.
Check that the battery is loaded properly.
Push the connector onto the pins (CON1) on the printed circuit board. (The connector is keyed for the correct polarity.)
Complete



4.5 Power Supply Units

4.5.1 Nomenclature

(1) A61P


Latch
For clipping the power supply to the base unit.
"POWER" LED
LED for indicating 5VDC power
Power fuse assembly
4A cartridge fuse for AC input power fitted in fuse holder.
Spare power supply fuse
Spare power supply fuse clipped to the rear of the terminal cover.
Terminal block
For details, see below. (Located under the terminal cover)
Terminal cover
Cover for terminal block. Remove during wiring.
Unit mounting hole
Allows the unit to be fixed to the base unit with an M4 (Metric thread) screw. (optional)
Terminal details
Power input terminals
Power input terminals for 100 or 200VAC. (See power supply specifications)
Input voltage select terminals
The input voltage must be specified with a jumper. When using the 100V range, connect the jumper accross the "SHORT AC100V" terminals. When using the 200V range, connect the jumper accross the "SHORT 200V" terminals.
LG terminal
Power filter ground.
FG terminal
Connected to printed circuit board shielding pattern.
All FG terminals on all equipment are connected internally.
(Safety Ground)
Terminal screw
M4 x 0.7 x 6 (Metric thread)
SPARE FUSE
INPUT AC100/200V
SHORT AC100V
SHORT AC200V
LG
FG

(2) A62P, A65P

Latch
For clipping the power supply to the base unit.

"POWER" LED
LED for indicating 5VDC power

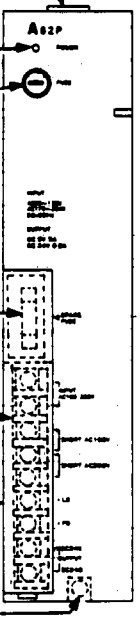
Power fuse assembly
4A cartridge fuse for AC input power fitted in fuse holder.

Spare power supply fuse
Spare power supply fuse clipped to the rear of the terminal cover.

Terminal block
For details, see below. (Located under the terminal cover)

Terminal cover
Cover for terminal block. Remove during wiring.

Unit mounting hole
Allows the unit to be fixed to the base unit with an M4 (Metric thread) screw. (optional)



Terminal details

Power input terminals
Power input terminals for 100 or 200VAC. (See power supply specifications)

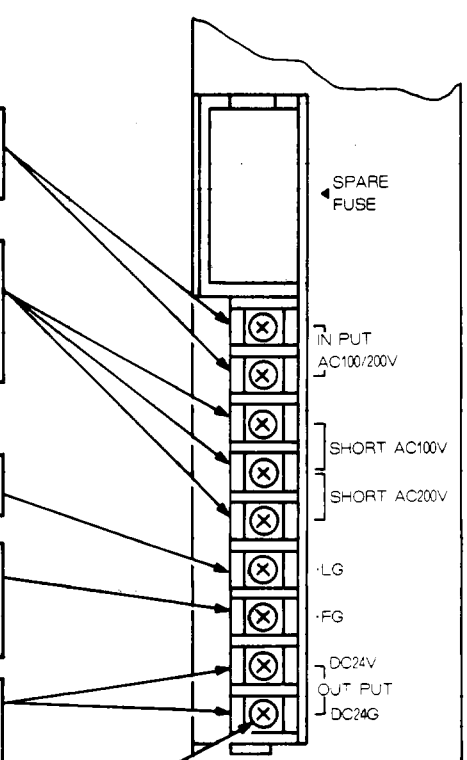
Input voltage select terminals
The input voltage must be specified with a jumper. When using the 100V range, connect the jumper accross the "SHORT AC100V" terminals. When using the 200V range, connect the jumper accross the "SHORT 200V" terminals.

LG terminal
Power filter ground.

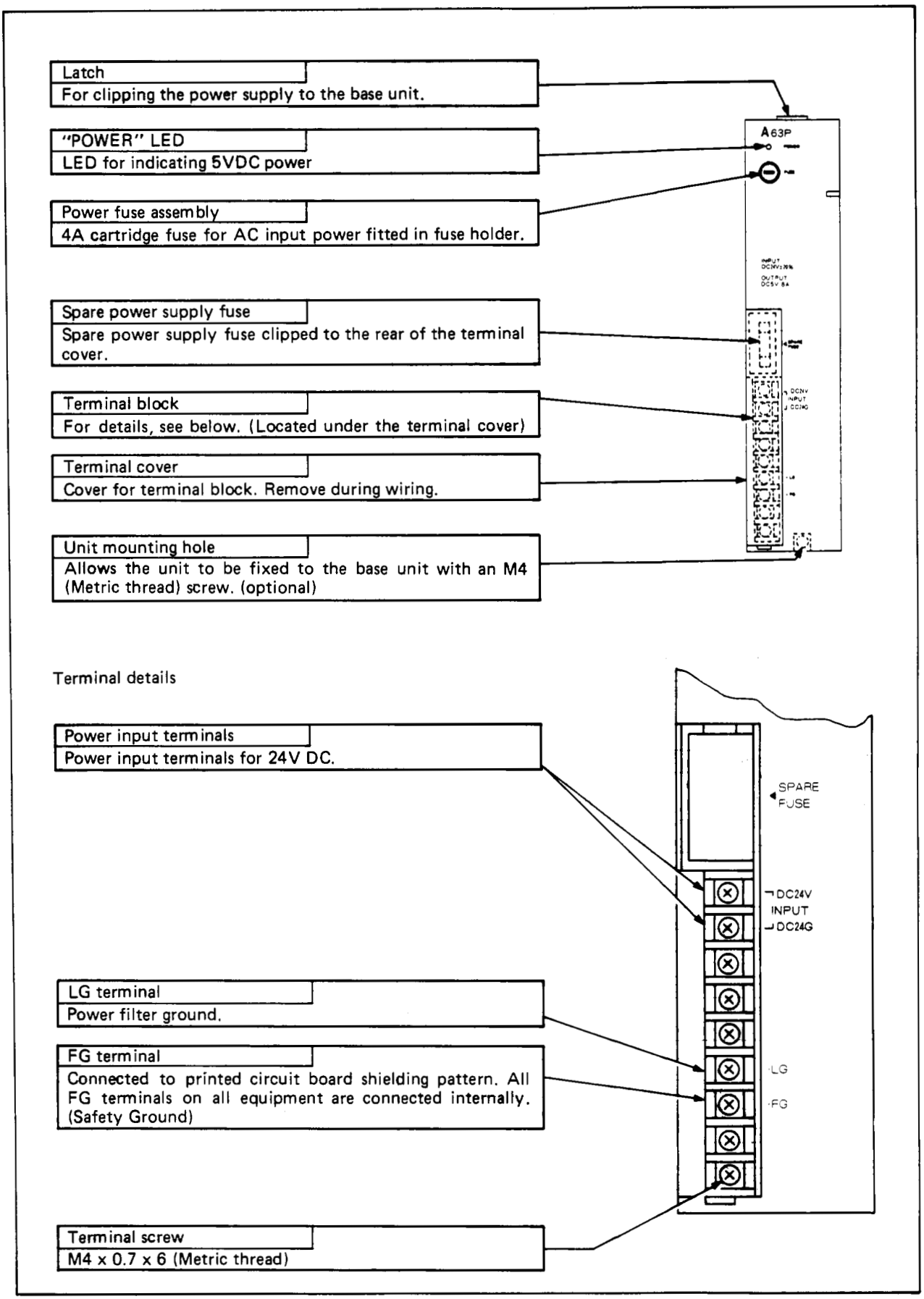
FG terminal
Connected to printed circuit board shielding pattern.
All FG terminals on all equipment are connected internally.
(Safety Ground)

24VDC, 24GDC output terminals
24VDC output used to supply certain I/O modules (e.g. relay output). All 24V wiring is external.

Terminal screw
M4 x 0.7 x 6 (Metric thread)



(3) A63P


Latch
For clipping the power supply to the base unit.
"POWER" LED
LED for indicating 5VDC power
Power fuse assembly
4A cartridge fuse for AC input power fitted in fuse holder.
Spare power supply fuse
Spare power supply fuse clipped to the rear of the terminal cover.
Terminal block
For details, see below. (Located under the terminal cover)
Terminal cover
Cover for terminal block. Remove during wiring.
Unit mounting hole
Allows the unit to be fixed to the base unit with an M4 (Metric thread) screw. (optional)
A63P
Terminal details
Power input terminals
Power input terminals for 24V DC.
LG terminal
Power filter ground.
FG terminal
Connected to printed circuit board shielding pattern. All FG terminals on all equipment are connected internally. (Safety Ground)
Terminal screw
M4 x 0.7 x 6 (Metric thread)
SPARE FUSE
DC24V
INPUT
DC24G
LG
FG

(4) A66P

Latch
For clipping the power supply to the base unit.

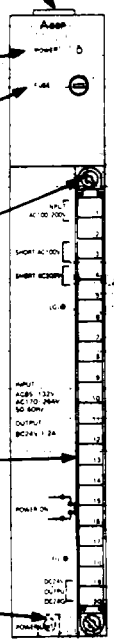
"POWER" LED
LED for indicating 5VDC power

Power fuse assembly
4A cartridge fuse for AC input power fuse holder fuse holder.

Terminal block fixing screw
Screw for installing and fixing the terminal block to the unit.

Terminal block
For details, see below. (Located under the terminal cover)

Unit mounting hole
Allows the unit to be fixed to the base unit with an M4 (Metric thread) screw. (optional)



Terminal details

Power input terminals
Power input terminals for 100 or 200VAC. (See power supply specifications)

Input voltage select terminals
The input voltage must be specified with a jumper. When using the 100V range, connect the jumper across the "SHORT AC100V" terminals. When using the 200V range, connect the jumper across the "SHORT 200V" terminals.

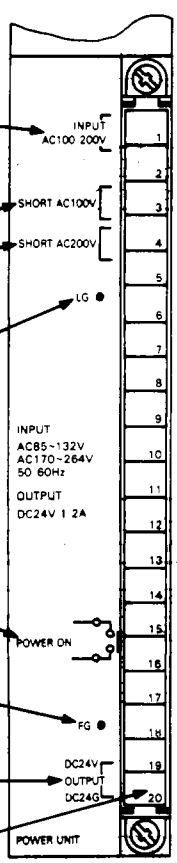
LG terminal
Power filter ground.

Power ON monitor contacts
Normally closed when the power supply is operating normally and giving 24VDC output.

FG terminal
Connected to printed circuit board shielding pattern. All FG terminals on all equipment are connected internally. (Safety Ground)

24V DC, 24GDC terminals
24V output supplied to appropriate I/O unit externally.

Terminal screw
M4 x 0.7 x 6 (Metric thread)



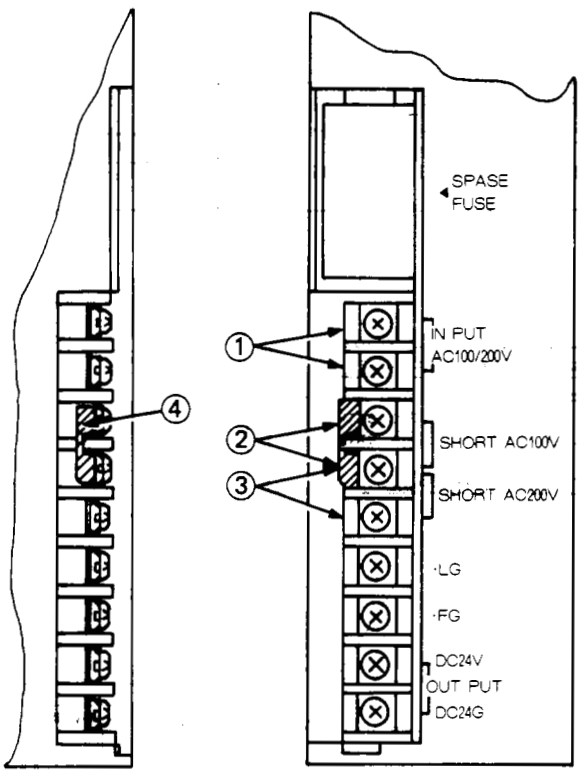
4.5.2 Power supply unit input voltage designation

The input voltage range, 100V or 200V, must be specified by placing a jumper (supplied) across two terminals as described below:

Remove the terminal cover from the power supply unit.

Remove the pair of terminal screws, ② or ③ , according to the supply voltage range used.
② : For the 100VAC range.
③ : For the 200VAC range.

Fit the jumper ④ , supplied with the power supply unit, as shown in the diagram on the right. In the illustration, the power supply has been designated as being in the 100VAC range.



POINT

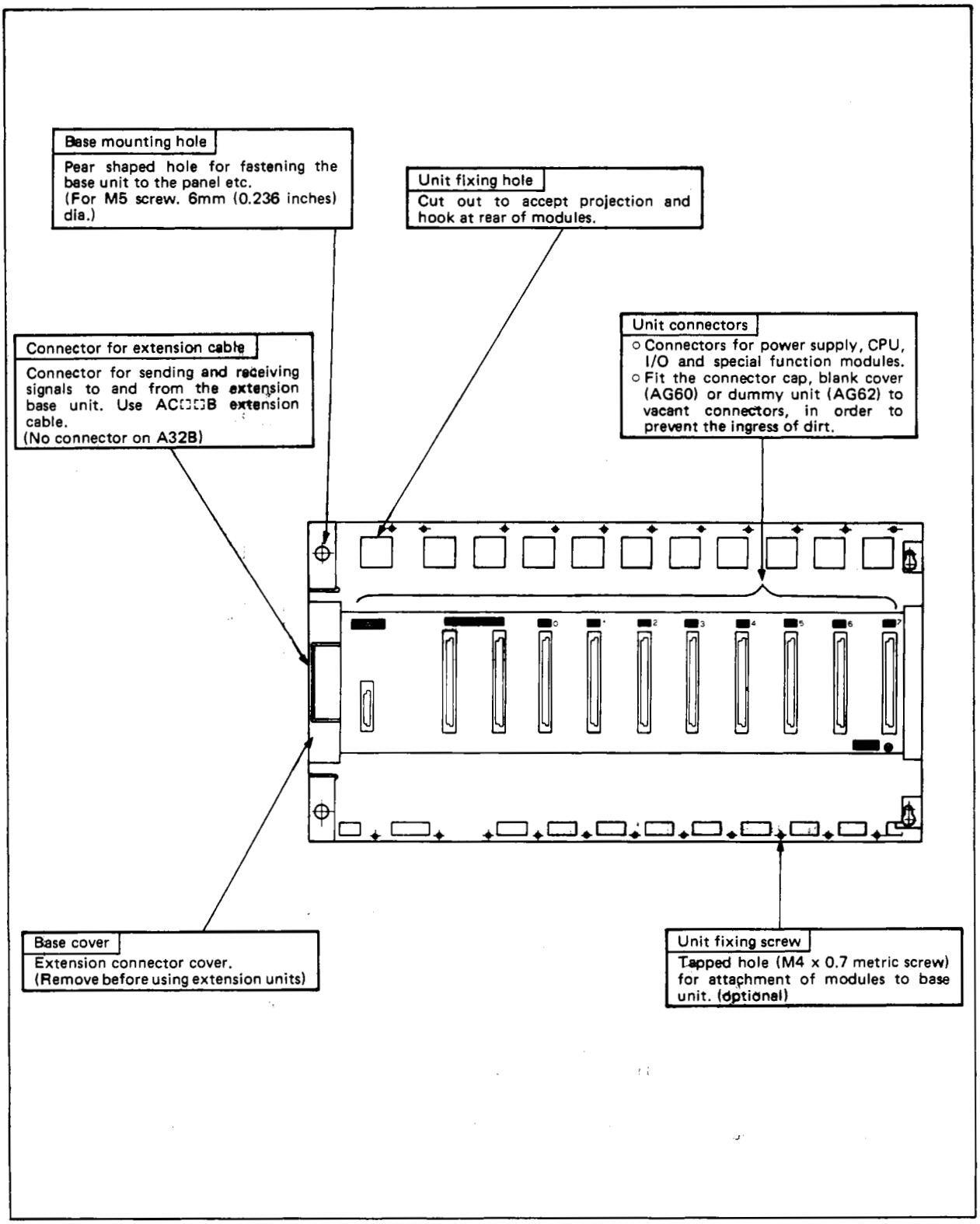
Wrong settings will lead to the following:

	Supply Line Voltage	
	100V AC	200V AC
Setting to 100V AC (Jumper setting ②)	–	The power supply is damaged.
Setting to 200V AC (Jumper setting ③)	The CPU does not operate. The power supply is not damaged.	–
No setting (Jumper not fitted)	The CPU does not operate. The power supply is not damaged.	

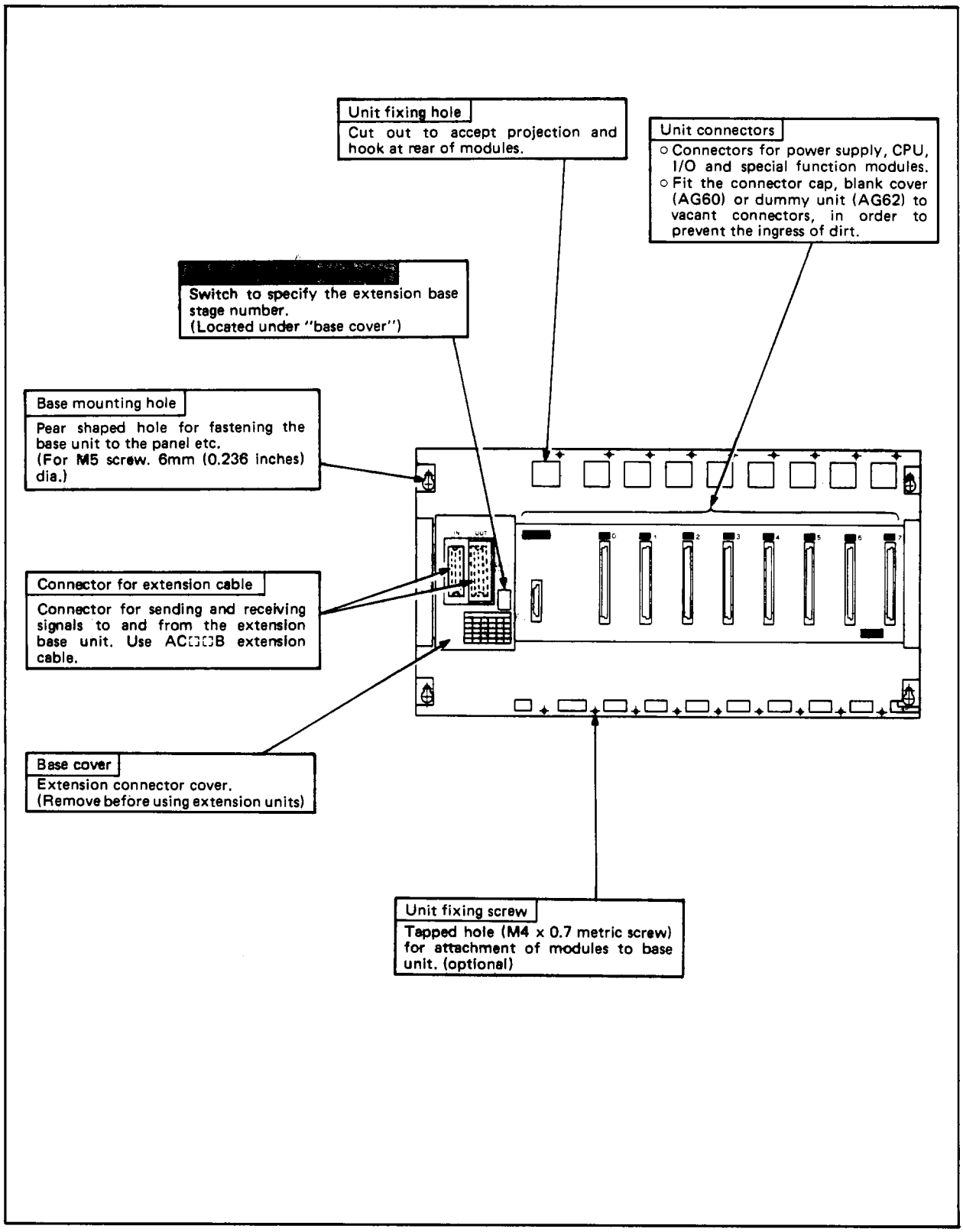
4.6 Base Units

4.6.1 Nomenclature

(1) Main base unit


Base mounting hole
Pear shaped hole for fastening the base unit to the panel etc. (For M5 screw. 6mm (0.236 inches) dia.)
Unit fixing hole
Cut out to accept projection and hook at rear of modules.
Connector for extension cable
Connector for sending and receiving signals to and from the extension base unit. Use AC□□B extension cable. (No connector on A32B)
Unit connectors
○ Connectors for power supply, CPU, I/O and special function modules.
○ Fit the connector cap, blank cover (AG60) or dummy unit (AG62) to vacant connectors, in order to prevent the ingress of dirt.
Base cover
Extension connector cover. (Remove before using extension units)
Unit fixing screw
Tapped hole (M4 x 0.7 metric screw) for attachment of modules to base unit. (optional)

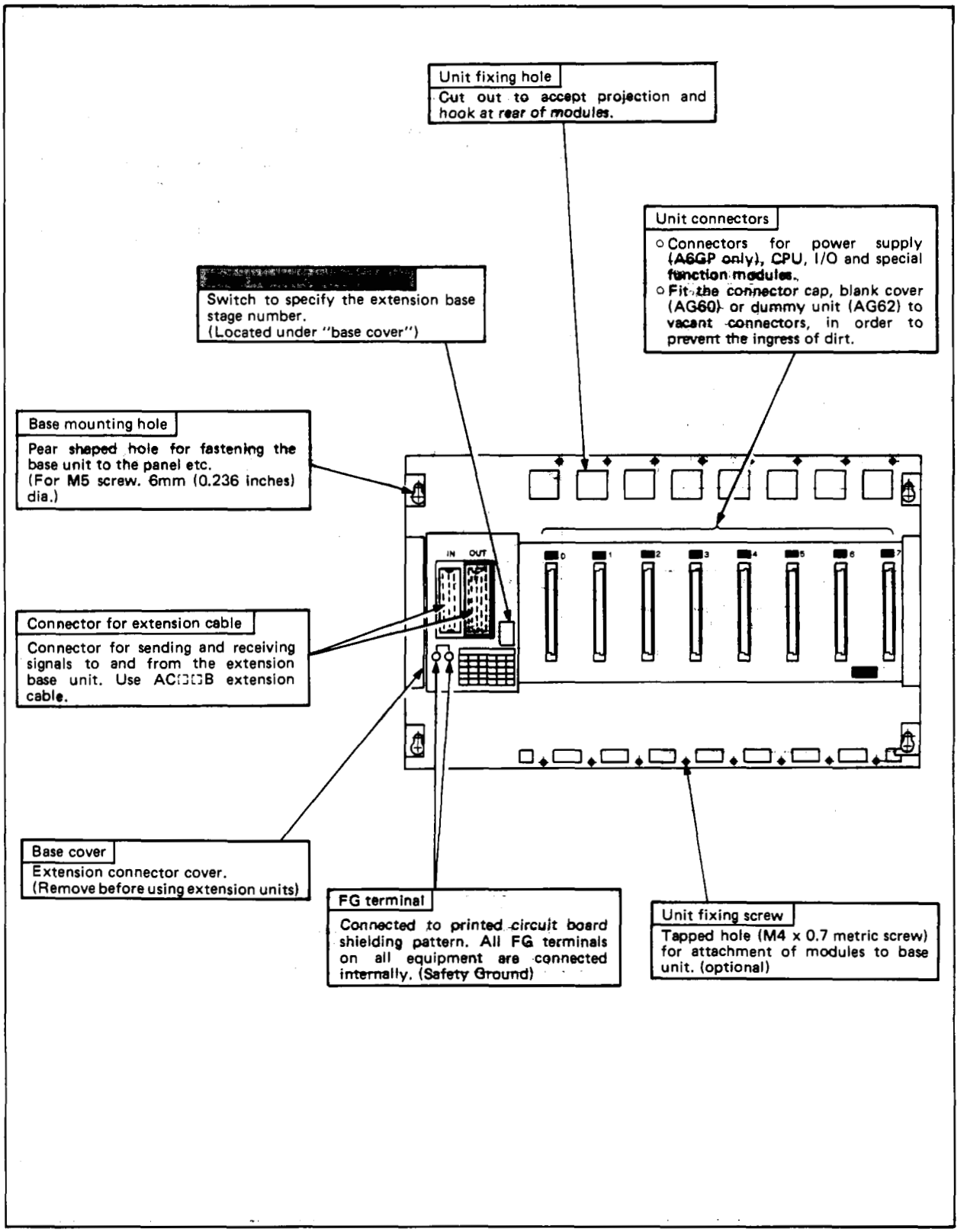
(2) Extension base units (A65B, A68B)


Unit fixing hole
Cut out to accept projection and hook at rear of modules.
Unit connectors
o Connectors for power supply, CPU, I/O and special function modules.
o Fit the connector cap, blank cover (AG60) or dummy unit (AG62) to vacant connectors, in order to prevent the ingress of dirt.
Switch to specify the extension base stage number.
(Located under "base cover")
Base mounting hole
Pear shaped hole for fastening the base unit to the panel etc.
(For M5 screw. 6mm (0.236 inches) dia.)
Connector for extension cable
Connector for sending and receiving signals to and from the extension base unit. Use AC□□B extension cable.
Base cover
Extension connector cover.
(Remove before using extension units)
Unit fixing screw
Tapped hole (M4 x 0.7 metric screw) for attachment of modules to base unit. (optional)

REMARKS

The shaded items require setting before using the unit.

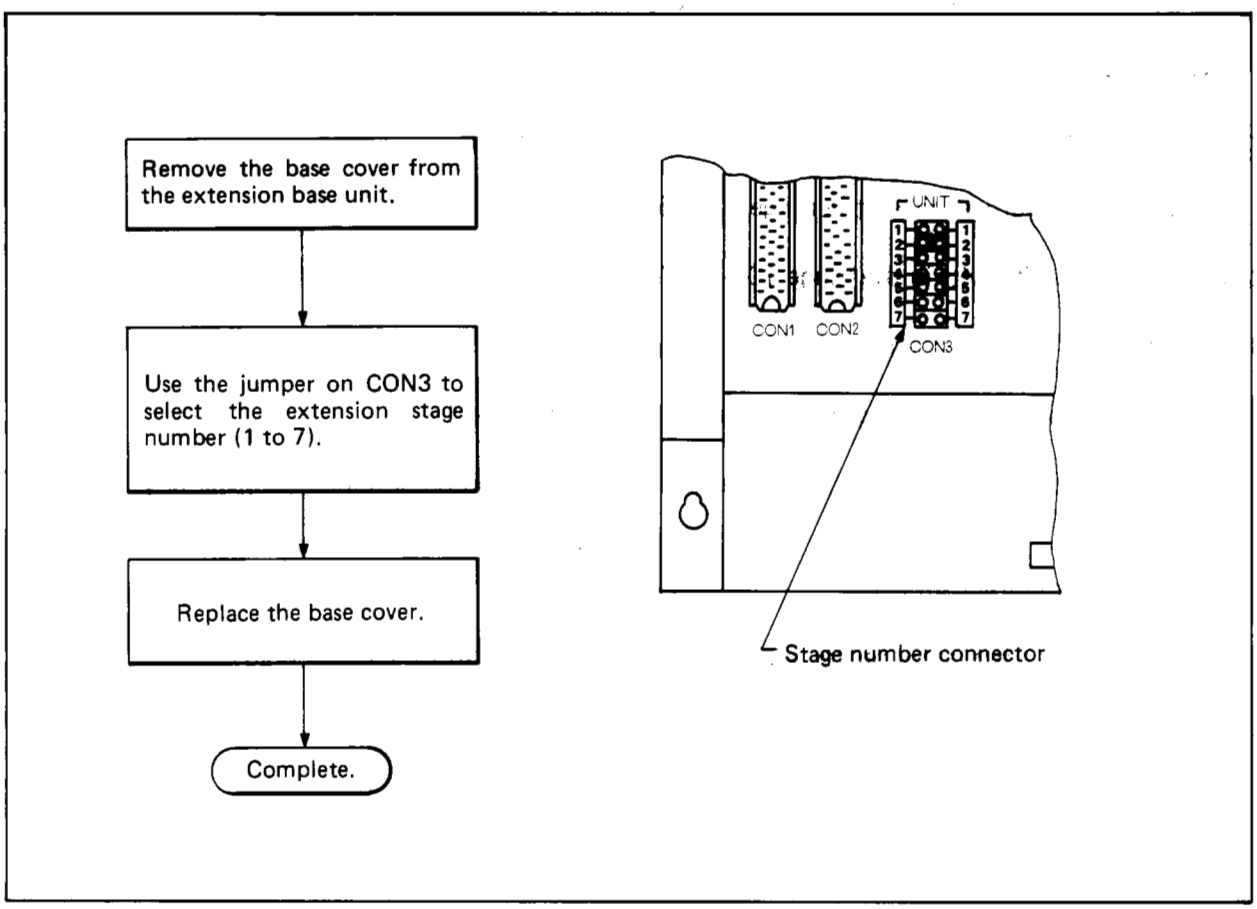
(3) Extension base units (A55B, A58B)


Unit fixing hole
Cut out to accept projection and hook at rear of modules.
Unit connectors
○ Connectors for power supply (A6GP only), CPU, I/O and special function modules.
○ Fit the connector cap, blank cover (AG60) or dummy unit (AG62) to vacant connectors, in order to prevent the ingress of dirt.
Switch to specify the extension base stage number.
(Located under "base cover")
Base mounting hole
Pear shaped hole for fastening the base unit to the panel etc.
(For M5 screw. 6mm (0.236 inches) dia.)
IN OUT
0 1 2 3 4 5 6 7
Connector for extension cable
Connector for sending and receiving signals to and from the extension base unit. Use AC□□B extension cable.
Base cover
Extension connector cover.
(Remove before using extension units)
FG terminal
Connected to printed circuit board shielding pattern. All FG terminals on all equipment are connected internally. (Safety Ground)
Unit fixing screw
Tapped hole (M4 x 0.7 metric screw) for attachment of modules to base unit. (optional)

REMARKS

The shaded items require setting before using the unit.

4.6.2 Extension stage number assignment



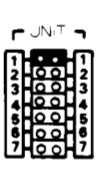
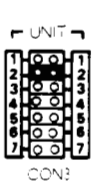
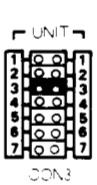
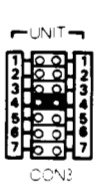
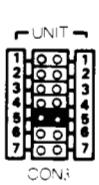
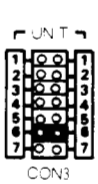
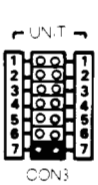
	Extension stage Number Setting						
	1st stage	2nd stage	3rd stage	4th stage	5th stage	6th stage	7th stage
Extension Stage Number Setting							

Table 4.4 Extension Base Stage Number Setting

POINT

Ensure that extension stage numbers have not been repeated or skipped.

5. LOADING AND INSTALLATION

The following instructions should be followed to ensure optimum performance:

5.1 Installation Environment

The PCs environment should meet the following specifications:

(1) Ambient temperature within the range 0 – 55°C.

(2) Ambient humidity within the range 10 – 90%RH.

(3) No condensation or sudden temperature changes.

(4) No corrosive or combustible gasses present in the atmosphere.

(5) No airborn conductive dust or debris (e.g. metal filings) and no conductive mists. (e.g. oil, salt, organic solvent)

(6) Protected from direct sunlight.

(7) Away from (or adequately protected from) strong power and/or magnetic fields.

(8) Protected from vibration and inpact.

5.2 Base Unit Mounting

5.2.1 Mounting instructions

(1) Leave a minimum of 80mm (3 inches) clearance above the PC to ensure proper ventilation and easy access. Fig. 5.1.

(2) The PC must not be installed on its side or horizontally as in Figs. 5.4 and 5.5.

(3) Ensure that the surface on which the base is to be mounted is flat to prevent possible flexing of the printed circuit boards.

(4) Do not mount the PC close to sources of vibration like large magnetic contactors or no-fuse breakers.

(5) Use wiring conduits where appropriate.
For installations with conduit running closer to the PC than the clearance distances shown in Figs. 1 and 2, note the following:

(a) When used above the PC, the conduit should be less than 50mm (2 inches) deep to allow proper ventilation and clearance for I/O module removal.

(b) When used below the PC, ensure that there is adequate clearance for cables, etc.

(6) All other equipment should be installed at least 100mm (4 inches) away from the PC to protect it from heat and noise.

5.2.2 Installation

To ensure optimum performance, install the unit according to the following guidelines:

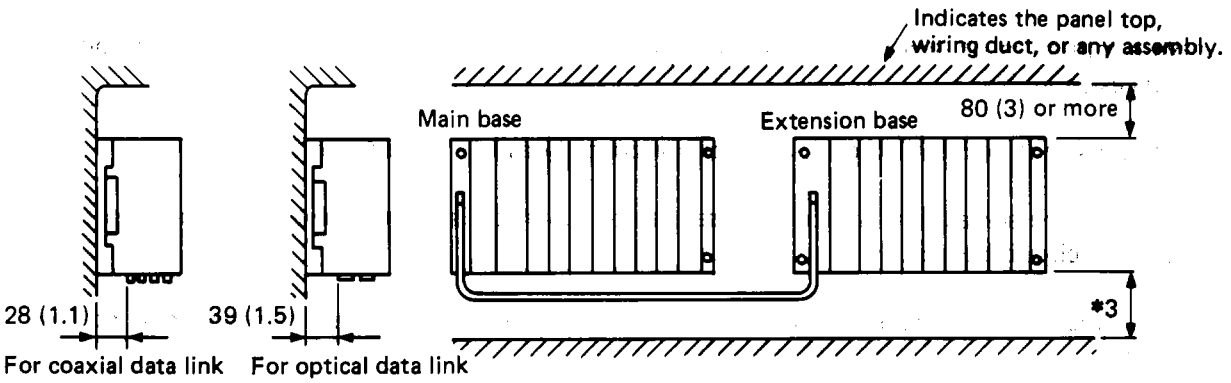
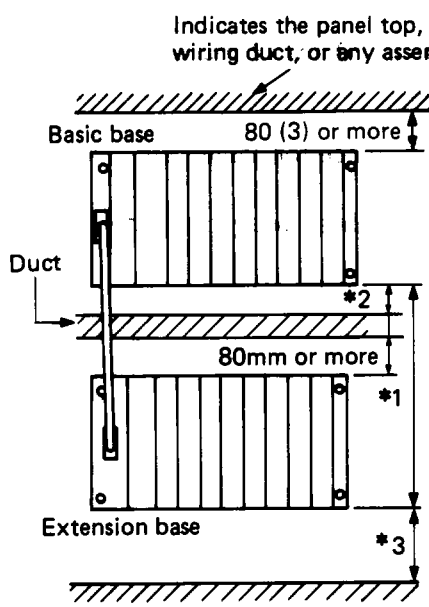


Fig. 5.1 Diagram showing minimum clearances Units : mm (inches)



*1: Depends on the length of the extension cable as indicated below.
450mm (17.7 inches) or less for Type AC06B cable
1050mm (41.3 inches) or less for Type AC12B cable
2850mm (112.2 inches) or less for Type AC30B cable

*2: 50mm (2 inches) or more when the link unit is not used.
100mm (4 inches) or more when 4.5mm (0.18 inch) dia. optical fiber cable or coaxial cable is used.
130mm (5.1 inches) or more when 8.5mm (0.33 inch) optical fiber cable is used.

*3: 50mm (2 inches) or more when the link unit is not used.
100mm (4 inches) or more when 4.5mm (0.18 inch) dia. optical fiber cable or coaxial cable is used.
130mm (5.1 inches) or more when 8.5mm (0.33 inch) optical fiber cable is used.

Fig. 5.2 Diagram showing minimum clearances

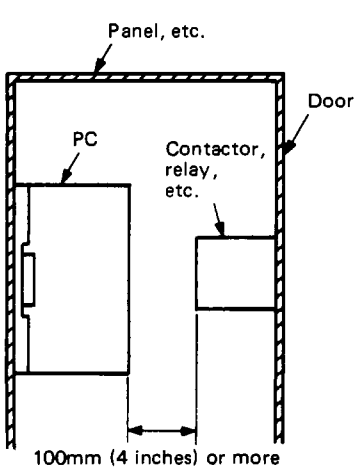


Fig. 5.3 Minimum Front Clearance with Panel Door Shut

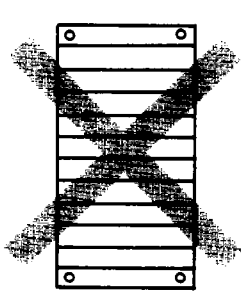


Fig. 5.4 Vertical Mounting (Not allowed)

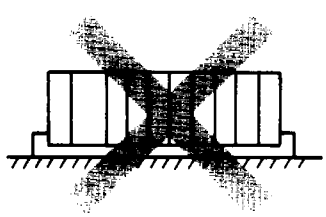


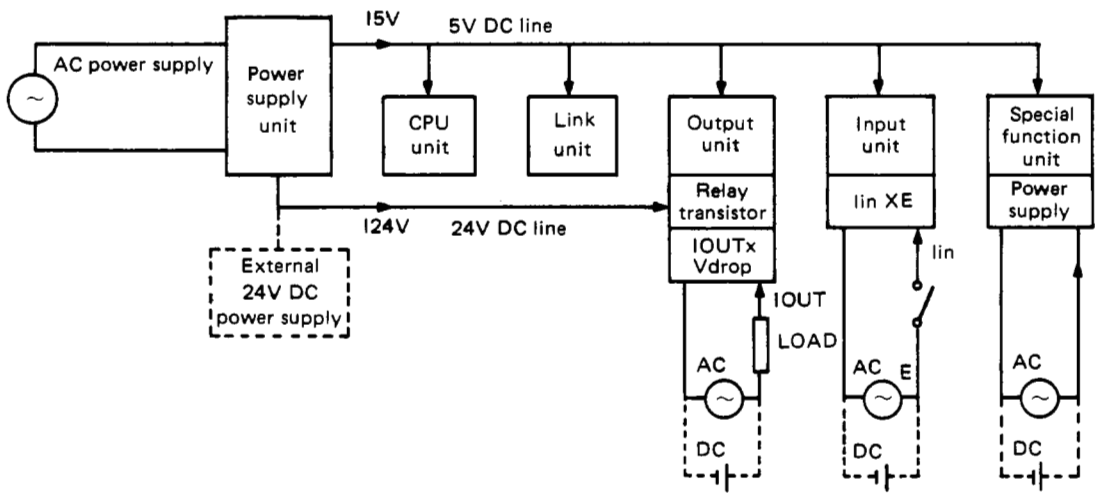
Fig. 5.5 Horizontal Mounting (Not allowed)

5.2.3 PC generated heat calculation

The operating ambient temperature of the PC must be kept below 55°C. The power generated by the PC should be dissipated by fans or similar and is calculated as follows:

Average power consumption

Power is consumed by the following PC areas:



(1) Power supply unit power consumption

Approximately 70% of the power supply unit current is converted into power with the remaining 30% dissipated as heat, i.e. 3/7 of the output power is used.

$$Wpw = \frac{3}{7} ((I5V \times 5) + (I24V)) \ (W)$$

where, I5V = 5V DC logic circuit current consumption of each unit
I24V = current consumption of the output units (with an average number of points switched on).....(Not for 24V input power supply units)

(2) Total 5V DC power consumption

5V is supplied to each unit via the base plate, this powers the logic circuitry.

$$W5V = I5V \times 5 \ (W)$$

(3) Total 24V DC output unit power consumption (with an average number of points switched on)

24V is supplied to drive output devices.

W24V = I24V x 24 (W)

(4) Power consumption of output circuits (with an average number of points switched on)

Wout = Iout x Vdrop x average number of outputs on at one time (W)

where, Iout = output current (actual operating current) (A)
Vdrop = voltage dropped across each output load (V)

(5) Power consumption of input circuits (with an average number of points switched on)

Win = Iin x E x average number of inputs on at one time (W)

where, Iin = input current (effective value for AC) (A)
E = input voltage (actual operating voltage) (V)

(6) Power consumption of the special function unit power supply is expressed as:

Ws = (I5V x 5) + (I24V x 24) + (I100V x 100) (W)

The sum of the above values is the power consumption of the entire PC system.

W = Wpw + W5V + W24V + Wout + Win + Ws (W)

Further calculations are necessary to work out the power dissipated by the other equipment in the panel.

Generally temperature rise in the panel is expressed as:

$$T = \frac{W}{UA} (°C)$$

where, W = power consumption of the entire PC system (obtained as above)
A = panel inside surface area (m^2)
U = 6 if the panel temperature is controlled by a fan, etc.
4 if panel air is not circulated.

POINT

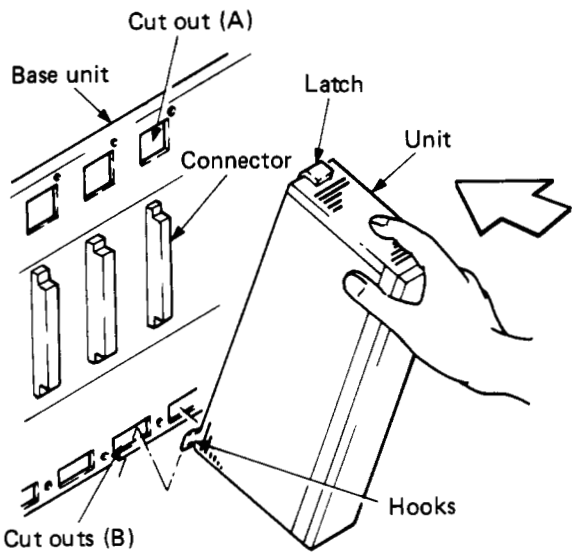
Fans, heat exchangers or cooling units must be installed if the panel temperature is likely to exceed 55°C.
Fans should be fitted with suitable filters and guards.

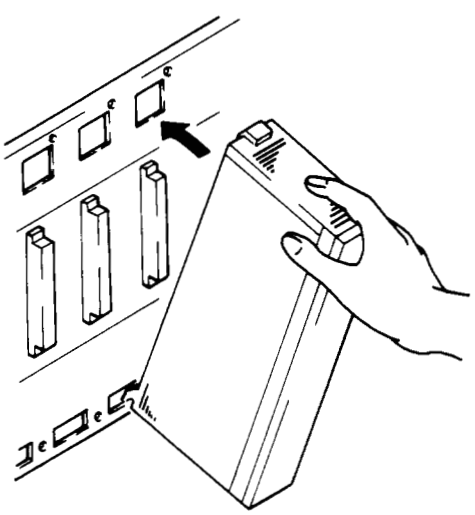
5.3 Installation and Removal of Rack Mounted Modules

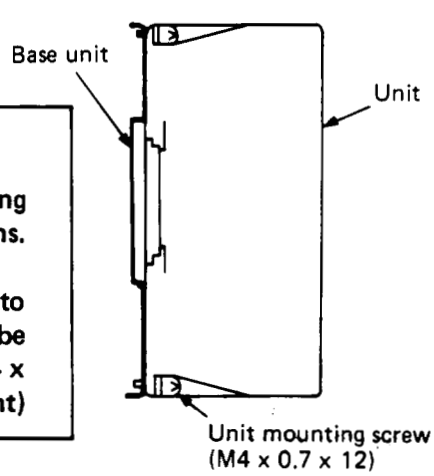
Install and remove modules from rack slots as follows:

(1) Installation

Fit the two hooks at the back of the unit into cut outs B in the base unit, and swing the module into place so that the white latch engages in cut out A.





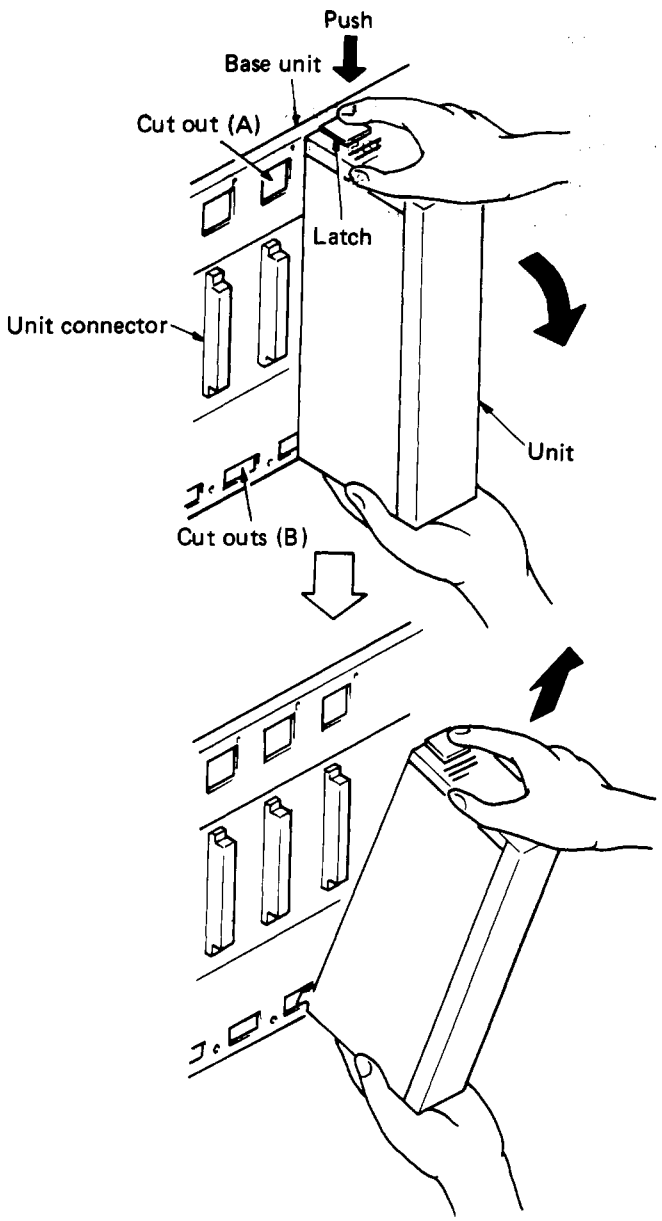


POINT

1. **Forcing the module into place without first locating the hooks in cut outs B will damage the connector pins.**
2. **When the completed system is liable to be subject to vibration and/or shock loads, each module may be screwed to the base unit for added security. Use M4 x 0.7 x 12 mm metric screws. (see diagram on the right)**

(2) Removal

Support the module with one hand and release the top white latch with the other, the module may then be swung out around the lower hooks and removed from the base unit.

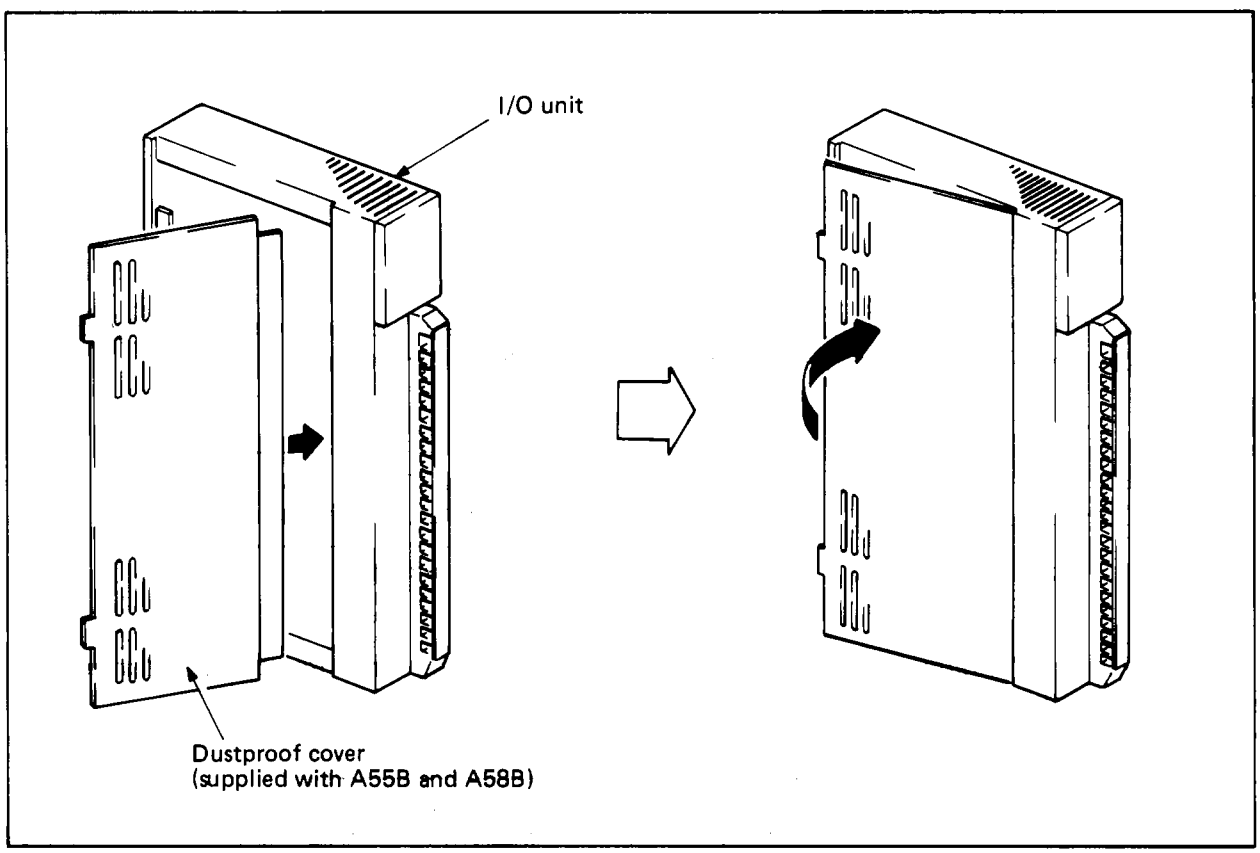


POINT

Pulling the module out of the rack without disengaging either the latch or the hooks will damage the plastic casing.

5.4 Installation of Dustproof Cover

When using an A55B or A58B (i.e. a base unit without a power supply), the module on the left hand end of the rack will require protection against the action of dust etc on its exposed printed circuit board. For this reason the "Dust proof cover" must be fitted as shown below:



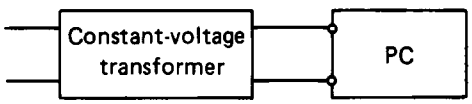
5.5 Wiring

The system should be wired according to the following guidelines.

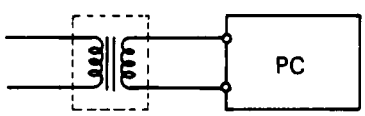
5.5.1 Wiring instructions

(1) Power supply wiring

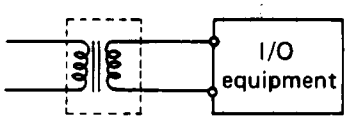
(a) A constant voltage transformer must be used if voltage fluctuations are outside the specified ranges. (See section 3.3.1)



(b) The PC is well protected against noise, however, an isolating transformer should be used if excessive noise is generated across the input terminals and/or ground.



Isolating transformer



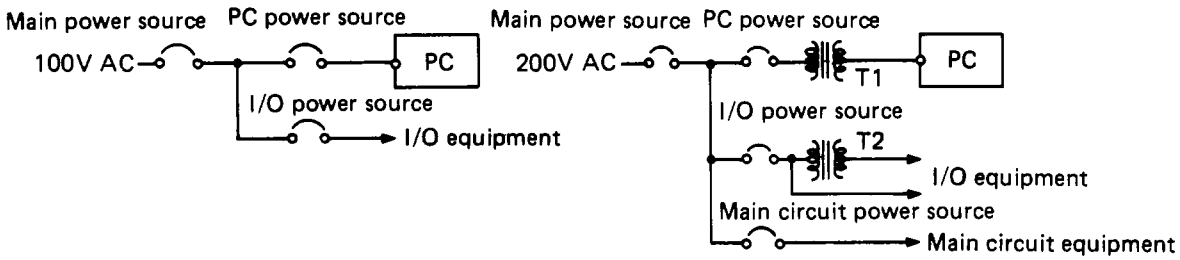
Isolating transformer

(c) Minimum VA ratings for step down (200V to 100V AC) power or isolating transformers are given in the following table.

Power Supply Unit	Min. transformer capacity
A1CPU	110VA x n
A61P	110VA x n
A62P	110VA x n
A65P	110VA x n
A66P	95VA x n

where n = number of power supply units.

(d) The PC, I/O equipment and all other equipment in the panel should be fed as shown below:

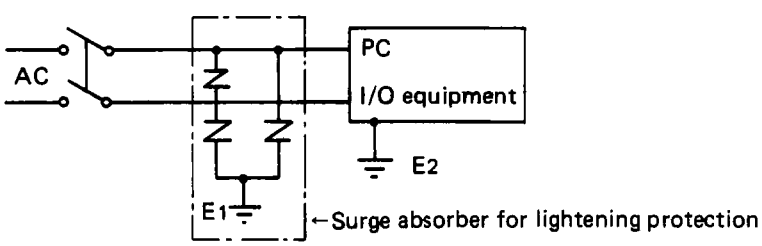


(e) 100V AC, 200V AC and 24V DC supply cables should be twisted and of the shortest possible length.

(f) Use the largest possible gauge (max. 2mm^2 (14 AWG)) for the 100V AC, 200V AC, and 24V DC cables to minimize any voltage drop.

(g) Do not bundle 100V AC and 24V DC cables with any main-circuit wiring or the I/O signal wires. Where possible, run input, output and supply wiring in separate ducts and keep them a minimum of 100mm (4 inches) apart.

(h) As a measure against any potential very large surges (e.g. due to lightening), use varistors as shown below.



POINT

1. **Ground the surge absorber (E1) and the PC (E2) separately.**
2. **When selecting a surge absorber make due allowance for increases in the power supply voltage.**

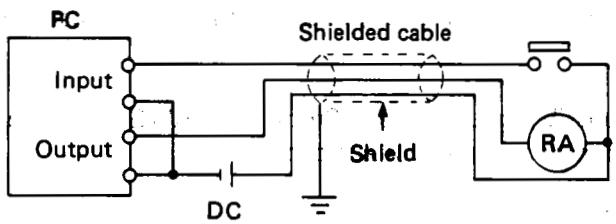
(2) Wiring of I/O equipment

(a) The I/O terminal blocks are designed for use with 0.75 (18 AWG) to 2mm² (14 AWG) gauge wire, 0.75mm² (18 AWG) being recommended for convenience.

(b) Bundle input and output lines separately.

(c) I/O signal wires must be at least 100mm (4 inches) away from high-voltage and large-current main circuit wiring.

(d) When the I/O signal wires cannot be separated from the main circuit wiring and/or the power supply wiring, use twested pair shielded cable grounded at one end only. (preferably the PC end).



(e) Where wiring runs through metal piping, ground the piping.

(f) Run the 24V DC I/O cables separately from 100V AC and 200V AC cables.

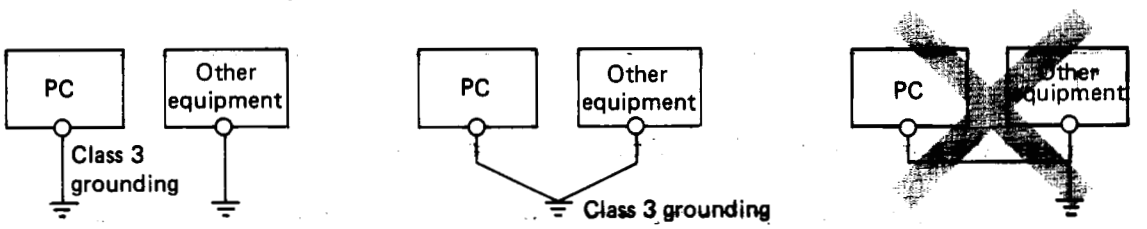
(g) Wiring over 200m (650ft) or further may give rise to leakage currents due to the line capacity, this may be corrected as discussed in Section 7.4.

(3) Ground

(a) Grounding is not necessary for the operation of the PC. Note the following, however, with reference to local regulations.

(b) Ground the PC independently from other equipment where possible. Class 3 grounding should be used (grounding resistance 100Ω or less).

(c) When independent grounding is impossible, use the grounding method shown below (2).

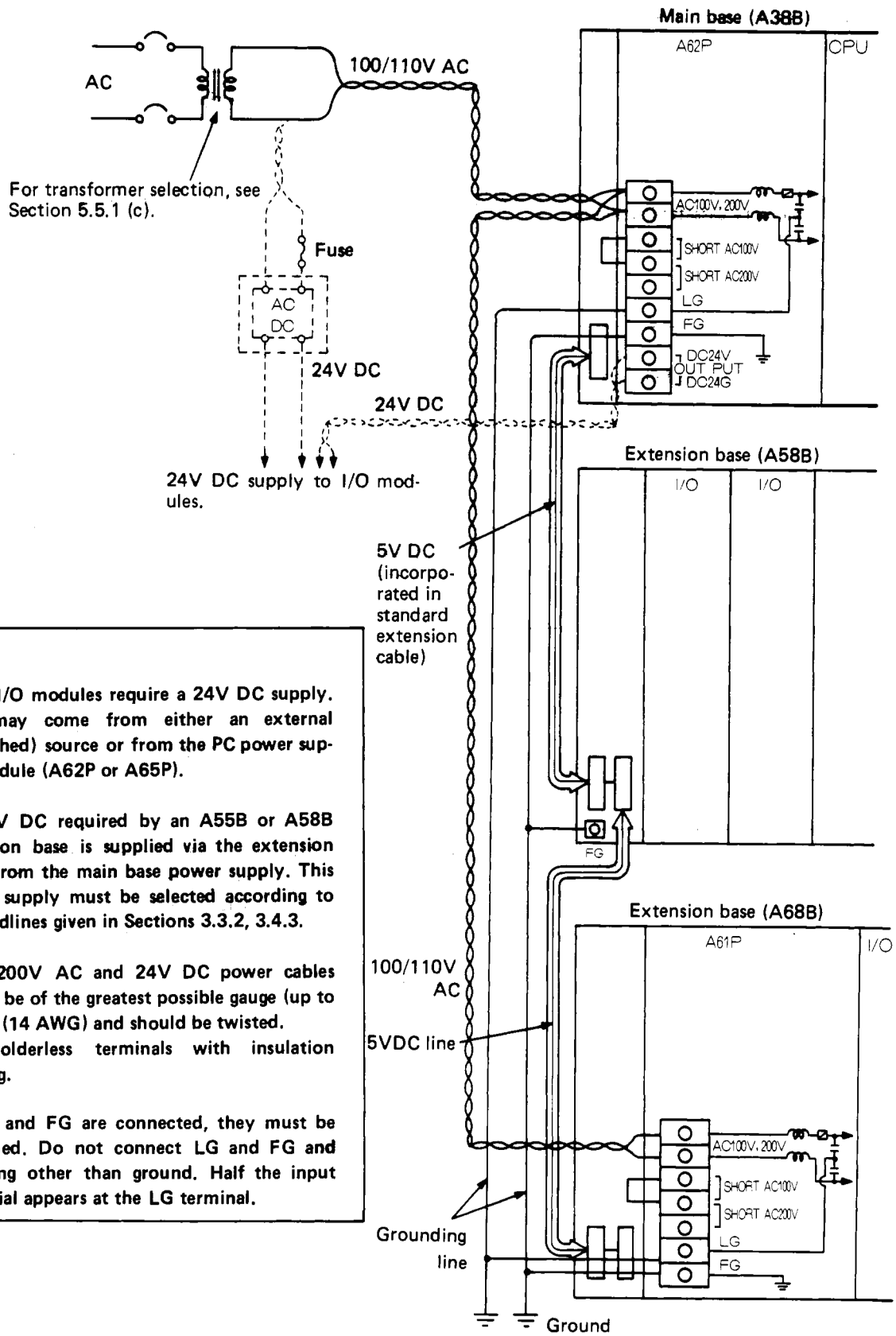


(1) Independent grounding . . . . . Best (2) Joint grounding . . . . . Good (3) Joint grounding . . . . . Not allowed

(d) Use 2mm² (14 AWG) (min.) grounding wire. The grounding points should be as near as possible to the PC to minimise the grounding cable length.

(e) Separate LG (power filter ground) and FG (frame ground, shield ground) terminals are provided and may be connected as appropriate. For optimum noise imunity, they should be independently connected to ground.

5.5.2 Power supply and grounding wiring example



POINT

1. Some I/O modules require a 24V DC supply. This may come from either an external (smoothed) source or from the PC power supply module (A62P or A65P).
2. The 5V DC required by an A55B or A58B extension base is supplied via the extension cable from the main base power supply. This power supply must be selected according to the guidlines given in Sections 3.3.2, 3.4.3.
3. 100V/200V AC and 24V DC power cables should be of the greatest possible gauge (up to 2mm^2 (14 AWG) and should be twisted. Use solderless terminals with insulation sleeving.
4. If LG and FG are connected, they must be grounded. Do not connect LG and FG and anything other than ground. Half the input potential appears at the LG terminal.

6. PRE-START-UP AND TEST PROCEDURES

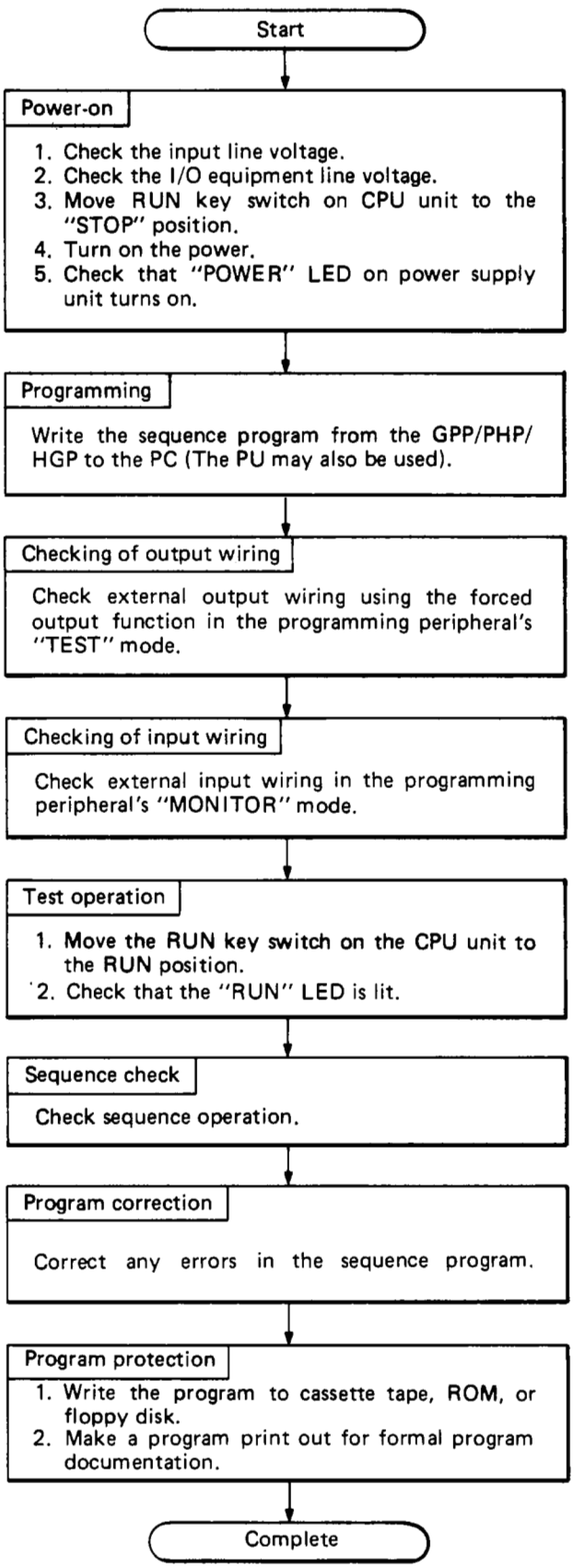
6.1 Pre-Test Check List

Item	Check	Description
1	Memory cassette installation and set-up	(1) Check that the memory cassette is securely fitted into the CPU unit. (2) Check that the user data matches the capacity of the memory cassette. (3) Check that the RAM/ROM setting is correct. (4) Check that RAM or ROM is correctly installed. (5) Check that the memory protect is ON (optional).
2	Battery installation	(1) Check that the battery lead wires are correctly connected to the memory cassette printed circuit board. (2) Check the battery voltage. (Nominal value: 3.6V)
3	Extension cable connection	(1) Check the main and extension base ends of the extension cables. (2) Check that the extension cable is connected to the correct connector.
4	Extension base stage number	(1) Check the extension stage number. (2) Check that extension stage numbers have not been repeated. (3) Check that extension stage numbers have not been skipped.
5	Module installation	(1) Check that valid modules have been installed in each base slot. (2) Where used, check that the I/O switch settings for the AG62 have been correctly set. (3) Check that the actual number of I/O points used is within the maximum I/O capacity of the PC CPU.
6	Fuse	(1) Check the fuse.
7	Power and I/O cable connection	(1) Check the cable connected to each terminal of each terminal block. (2) Check the terminal screws on the power supply and I/O units. (3) Check that wire gauges are within specification.

Table 6.1 Check List

6.2 Test Procedure

After completing the pre-test check list given in the previous section, carry out the following test procedure.


Start
Power-on
1. Check the input line voltage.
2. Check the I/O equipment line voltage.
3. Move RUN key switch on CPU unit to the "STOP" position.
4. Turn on the power.
5. Check that "POWER" LED on power supply unit turns on.
Programming
Write the sequence program from the GPP/PHP/HGP to the PC (The PU may also be used).
Checking of output wiring
Check external output wiring using the forced output function in the programming peripheral's "TEST" mode.
Checking of input wiring
Check external input wiring in the programming peripheral's "MONITOR" mode.
Test operation
1. Move the RUN key switch on the CPU unit to the RUN position.
2. Check that the "RUN" LED is lit.
Sequence check
Check sequence operation.
Program correction
Correct any errors in the sequence program.
Program protection
1. Write the program to cassette tape, ROM, or floppy disk.
2. Make a program print out for formal program documentation.
Complete

7. TROUBLESHOOTING

7.1 Basic Troubleshooting

(1) Visual checks

Check the following.

1) The physical action or motion of the process being controlled (in STOP and RUN status)

2) Power supply, on or off, intermittent failure

3) Status of I/O equipment

4) Condition of wiring (I/O wires, cables)

5) Display states of various indicators (e.g. POWER, RUN, and I/O LEDs, etc.)

6) Switch settings (e.g. extension base, memory protect, etc.)

After completing the visual checks, connect the peripheral programming unit and monitor the status of the PC and the program.

(2) Reset check

Observe any changes in the error condition during the following:

1) Set the RUN key switch to the "STOP" position.

2) Reset the CPU (with the RESET key switch).

3) Turn the power off and on.

(3) Narrow down the possible causes of the problem and try to deduce where the fault lies, i.e:-

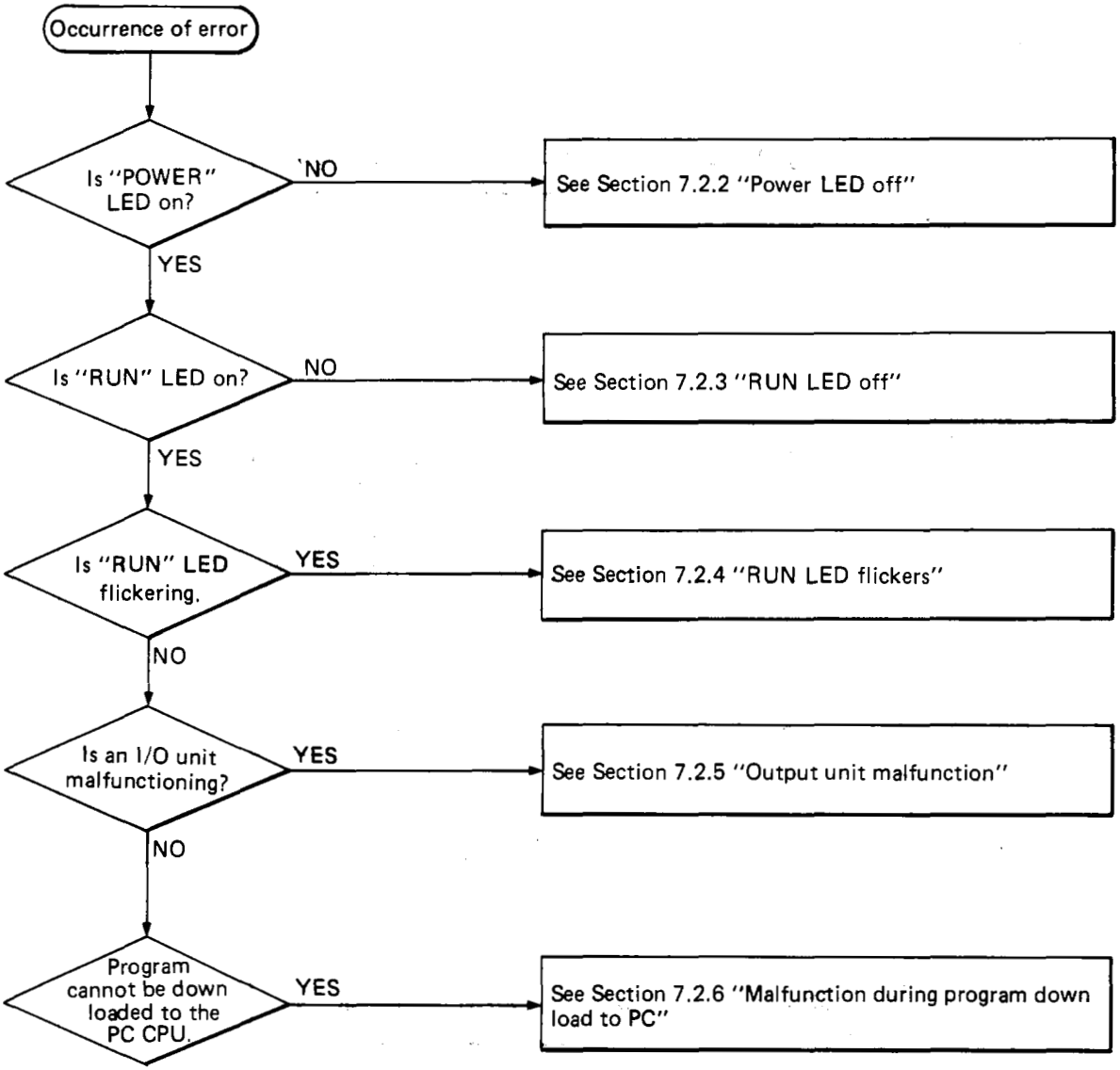
1) Inside or outside the PC.

2) I/O unit or otherwise.

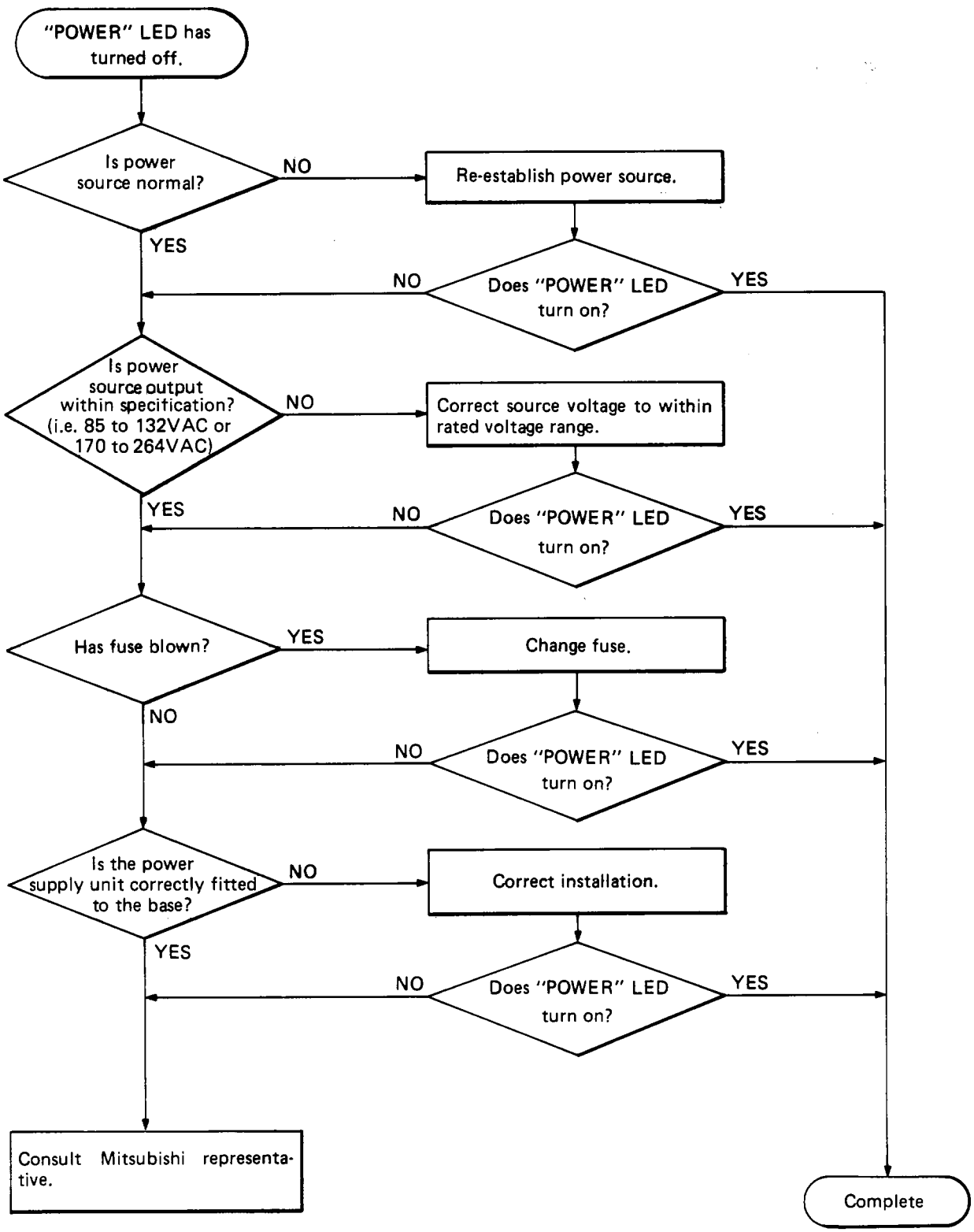
3) Sequence program.

7.2 Detailed Troubleshooting

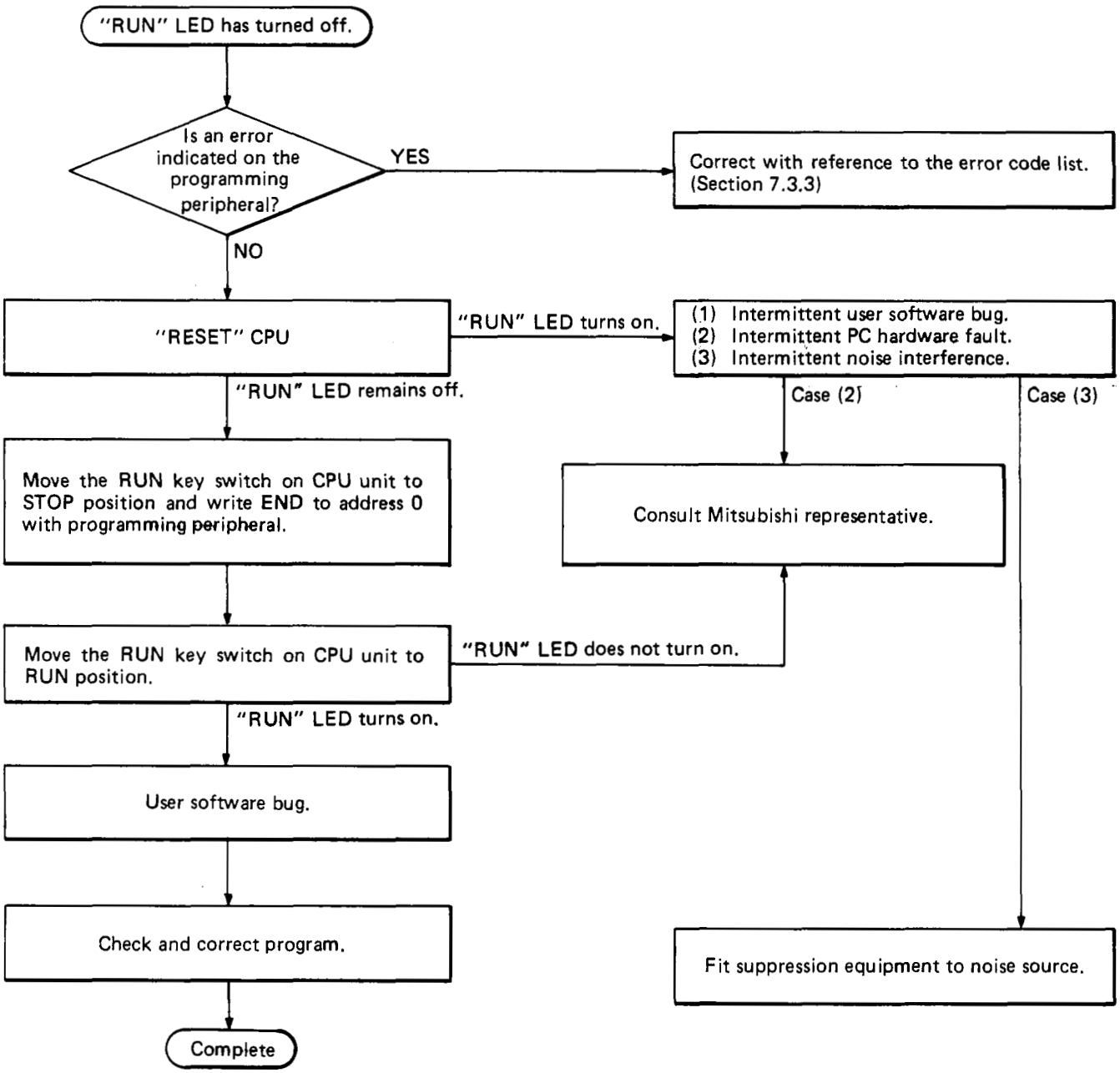
7.2.1 Troubleshooting flow charts



7.2.2 Power LED off

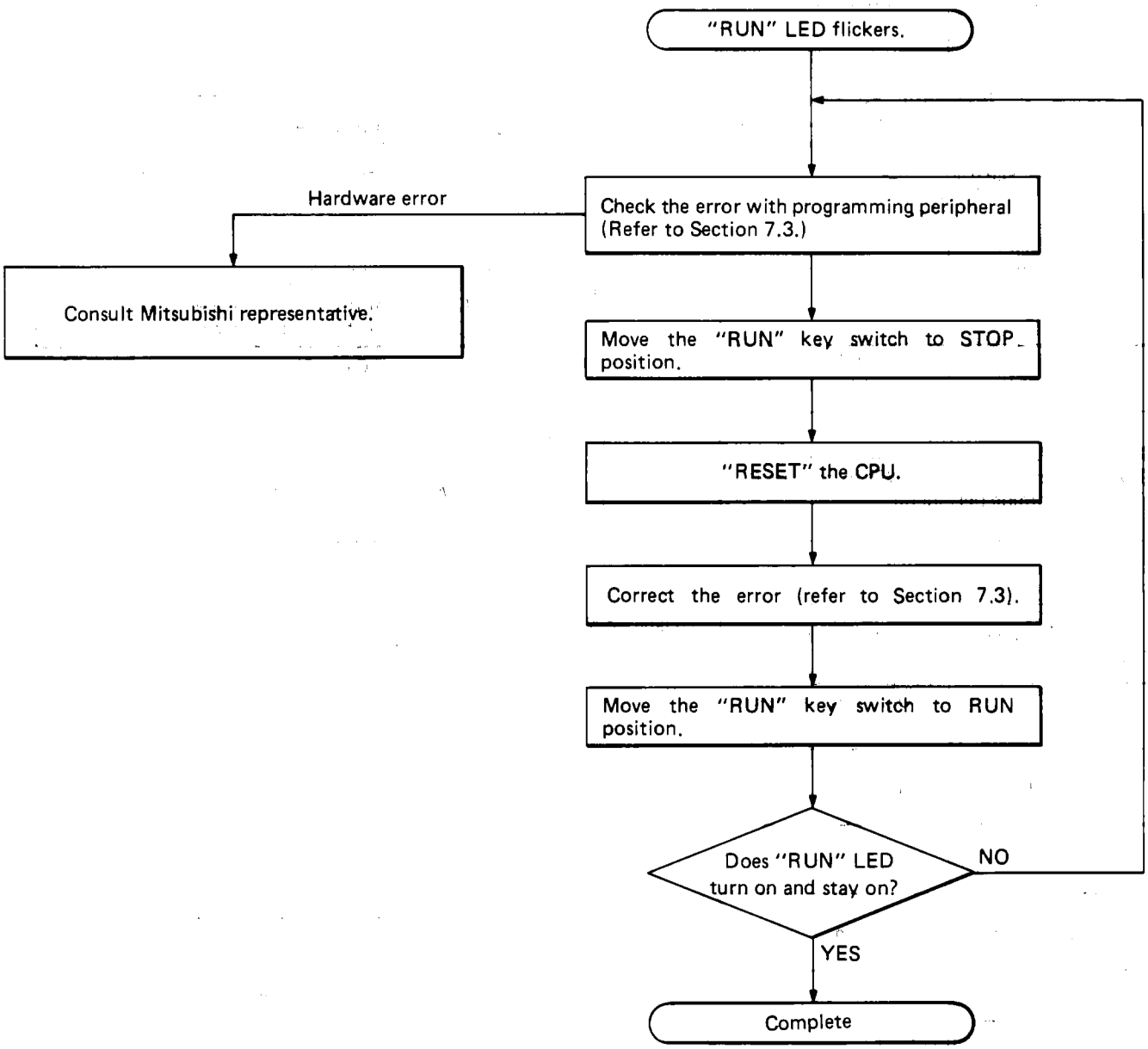


7.2.3 RUN LED off


"RUN" LED has turned off.
Is an error indicated on the programming peripheral?
YES
Correct with reference to the error code list. (Section 7.3.3)
NO
"RESET" CPU
"RUN" LED turns on.
(1) Intermittent user software bug.
(2) Intermittent PC hardware fault.
(3) Intermittent noise interference.
"RUN" LED remains off.
Case (2)
Case (3)
Move the RUN key switch on CPU unit to STOP position and write END to address 0 with programming peripheral.
Consult Mitsubishi representative.
Move the RUN key switch on CPU unit to RUN position.
"RUN" LED does not turn on.
"RUN" LED turns on.
User software bug.
Check and correct program.
Fit suppression equipment to noise source.
Complete

7.2.4 RUN LED flickers

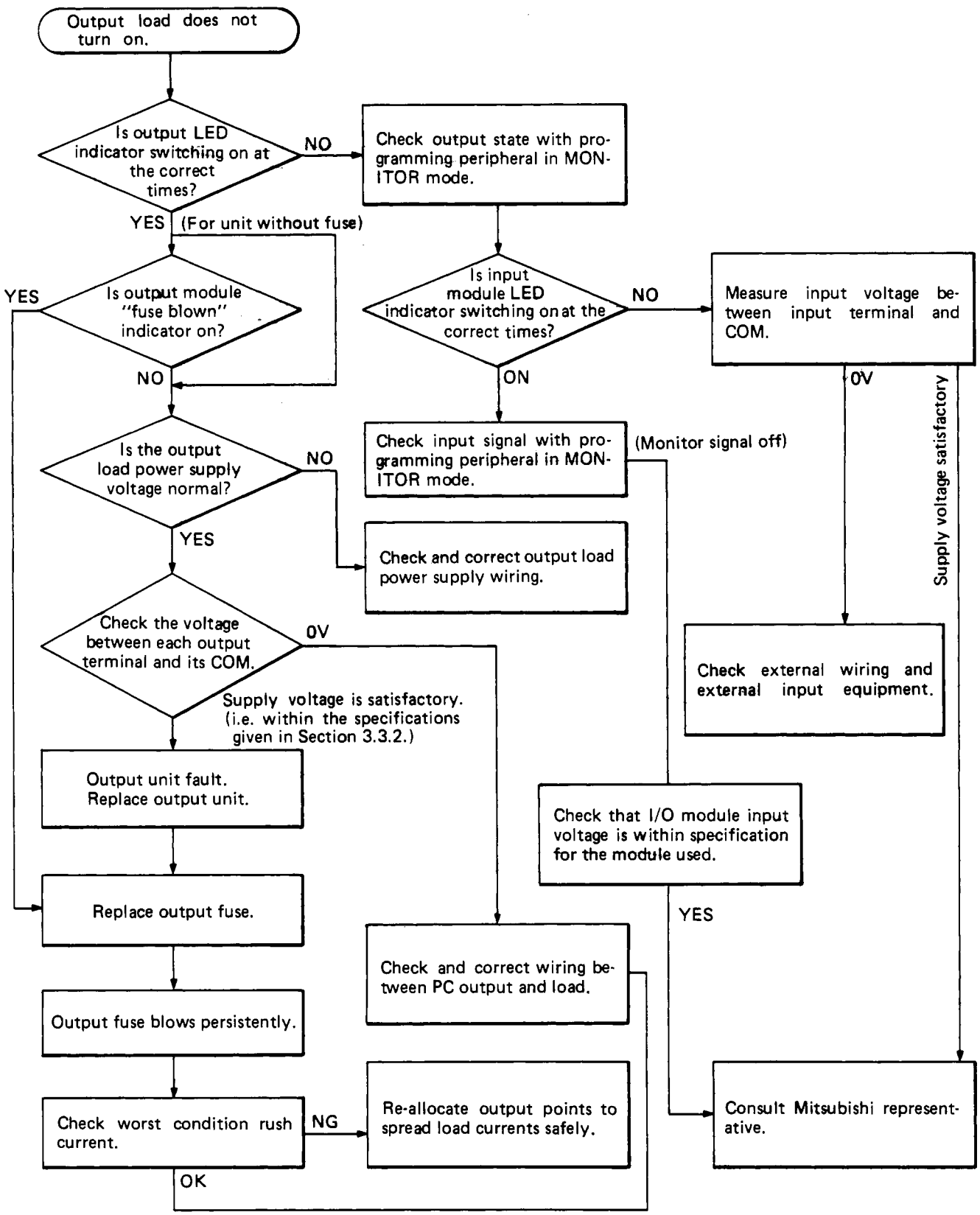
The A3HCPU is fitted with an ASCII character display which will indicate any error which has caused the RUN LED to flicker.


"RUN" LED flickers.
Check the error with programming peripheral (Refer to Section 7.3.)
Hardware error
Consult Mitsubishi representative.
Move the "RUN" key switch to STOP position.
"RESET" the CPU.
Correct the error (refer to Section 7.3).
Move the "RUN" key switch to RUN position.
Does "RUN" LED turn on and stay on?
NO
YES
Complete

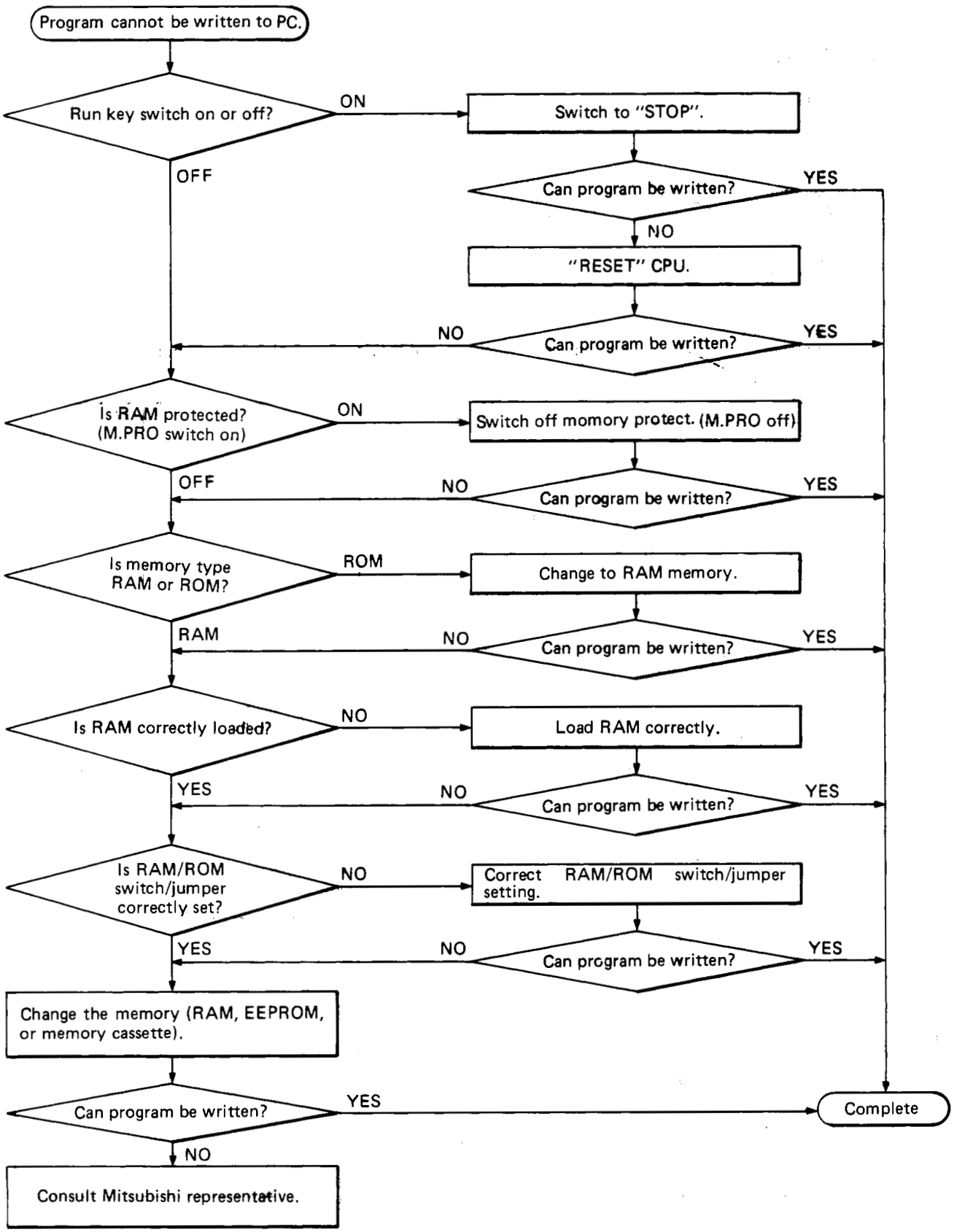
POINT

The error condition which causes the RUN LED to flicker, is latched so that when the PC is switched to STOP status, the RUN LED will continue to flicker. It may be cleared by resetting the CPU.

7.2.5 Output unit malfunction


Output load does not turn on.
Is output LED indicator switching on at the correct times?
NO
Check output state with programming peripheral in MONITOR mode.
YES
(For unit without fuse)
Is input module LED indicator switching on at the correct times?
NO
Measure input voltage between input terminal and COM.
YES
Is output module "fuse blown" indicator on?
NO
ON
0V
Supply voltage satisfactory
Check input signal with programming peripheral in MONITOR mode.
(Monitor signal off)
Is the output load power supply voltage normal?
NO
YES
Check and correct output load power supply wiring.
Check the voltage between each output terminal and its COM.
0V
Check external wiring and external input equipment.
Supply voltage is satisfactory. (i.e. within the specifications given in Section 3.3.2.)
Output unit fault. Replace output unit.
Check that I/O module input voltage is within specification for the module used.
Replace output fuse.
YES
Check and correct wiring between PC output and load.
Output fuse blows persistently.
Check worst condition rush current.
NG
Re-allocate output points to spread load currents safely.
Consult Mitsubishi representative.
OK

7.2.6 Malfunction in program down load to PC



7.3 Error Code List

The procedures for reading an error code from the CPU are shown below:

7.3.1 Reading of error codes

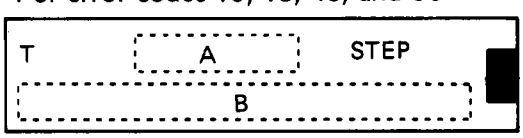
Procedures for the different programming peripherals are shown below.

(1) PU

Press the following keys: [TEST] [DEC K] [STP +] or [TEST] [DEC K] [STP −]

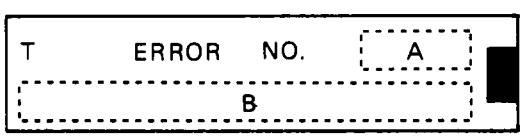
The following display results:

- For error codes 10, 13, 46, and 50



A: Error step number (Maximum of 5 digits)
B: Error message

- For all other error codes

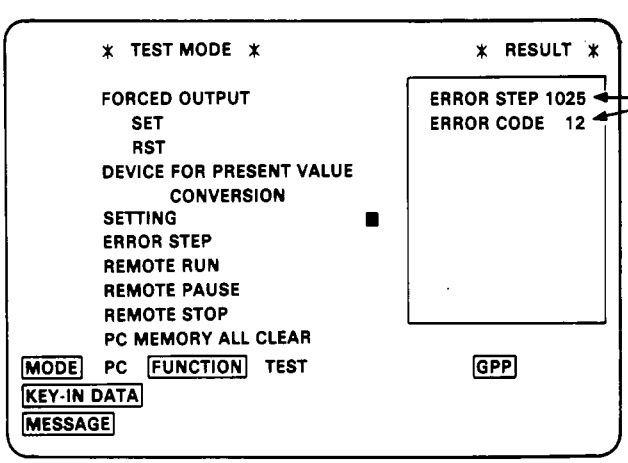


A: Error code
B: Error message

(2) GPP/PHP/HGP

Operation [PC] [TEST] [↓] ------- [↓] [GO]

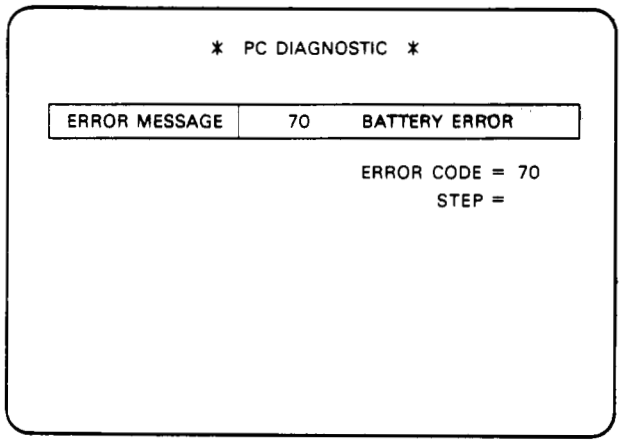
Move the cursor to "error step" and press [GO], the error code (together with its step number where appropriate) is indicated in the result column as shown below:



For further error diagnosis (for codes other than 10, 15, 46, and 50) procede as follows:—

Press the following keys: LST MNT ↓ ---------- GO

→ Move the cursor to "PC DIAGNOSTICS".

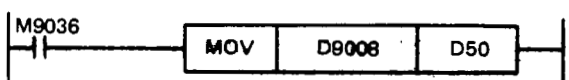


The content of special register D9008 may also be monitored to give the error code.

7.3.2 Error code retention during power failure

When it is necessary to store an error code which appears in D9008, (e.g. for reading back after a power failure or CPU reset) the error code may be written to a latched data register or file register as shown in the example below:

Example



In order for the error code to be retained after power failure or CPU reset, D50 must be set as latching in the PC parameters and the battery must be connected.

7.3.3 Error code list

Error codes are generated as follows:

Error Message	Content of Special Register D9008 (BIN value)	Resulting CPU Status	Error and Cause	Corrective Action
"INSTRCT." CODE ERR" (Checked during instruction execution)	10	Stop	An unrecognized instruction code is being used. (1) An invalid ROM has been loaded. (2) Program editing has corrupted a program step.	(1) Examine the program step indicated by the diagnostics and correct. (2) Correct or replace the ROM where appropriate.
"PARAMETER ERROR" (Checked at power-on, STOP → RUN, and PAUSE → RUN)	11	Stop	(1) The parameter memory capacity exceeds the allowed CPU memory capacity. (2) Parameter data has been corrupted (by noise or installation of memory cassette with PC power on).	(1) Check and correct memory capacity. (2) Check that PC memory is correctly installed. (3) Check and correct PC parameter data.
"MISSING END INS." (Checked at STOP → RUN)	12	Stop	(1) There is no END (FEND) instruction in the program. (2) Subprogram has been allocated in the parameters and this has no END instruction.	(1) Write END in program/subprogram.
"CAN'T EXECUTE (P)" (Checked at the execution of instruction)	13	Stop	(1) No jump destination or several destinations specified for the [CJ], [SCJ], [CALL], [CALLP], or [JMP] instruction. (2) [CHG] instruction and no subprogram. (3) The [RET] instruction has been executed with no corresponding [CALL] instruction. (4) [CJ], [SCJ], [CALL], [CALLP], or [JMP] has been executed with jump destination located after the END instruction.	(1) Examine the program step indicated by the diagnostics and correct.

Table 7.1 Error Code List

Error Message	Content of Special Register D9008 (BIN value)	Resulting CPU Status	Error and Cause	Corrective Action
"CAN'T EXECUTE (I)" (Checked at the occurrence of interruption)	15	Stop	(1) No interrupt pointer I, corresponding to interrupt input; or interrupt pointer used several times. (2) No [IRET] instruction in the interrupt program. (3) Incorrect use of [IRET] instruction outside the interrupt program.	(1) Check and correct interrupt program associated with the interrupt signal received. (2) Check and correct use of [IRET] instruction inside or outside interrupt program.
"CASSETTE ERROR" (Checked at power-on)	16	Stop	The memory cassette is not loaded.	Load the memory cassette and reset.
"RAM ERROR" (Checked at power-on)	20	Stop	(1) The PC CPU cannot access the data memory area of the PC.	Possible hardware fault, consult Mitsubishi representative.
"OPE. CIRCUIT ERR." (Checked at power-on)	21	Stop	(1) Invalid PC sequence program.	Examine and correct PC sequence program.
"WDT ERROR" (Checked at the execution of END instruction)	22	Stop	Scan time exceeds watch dog error monitor time. (1) User program scan time has increased. (2) Instantaneous power failure during program scan has caused apparent scan time to increase.	(1) Check PC program scan time and reduce using [CJ] instruction. (2) Check for instantaneous power failures by monitoring special register D9005.
"SUB-CPU ERROR" (Checked continuously)	23 (During run) 26 (At power-on)	Stop	Hardware fault.	Consult Mitsubishi representative.
"END NOT EXECUTE" (Checked at end of program)	24	Stop	(1) The END instruction has been missed (e.g. memory cassette removed during program execution). (2) The END instruction has been corrupted.	(1) Reset CPU. If error persists, possible hardware fault, consult Mitsubishi representative.
"WDT ERROR" (Checked continuously)	25	Stop	Hardware fault.	Consult Mitsubishi representative.

Table 7.1 Error Code List (Continued)

Error Message	Content of Special Register D9008 (BIN value)	Resulting CPU Status	Error and Cause	Corrective Action
"UNIT VERIFY ERR." (Checked continuously)	31	Run (Stop)	An I/O module (including special function module) has been removed from the base unit while the P.C. power is switched on.	Examine special data registers D9116 to D9123 to establish which I/O unit has been removed. Correct and reset CPU.
"FUSE BREAK OFF" (Checked continuously)	32	Run (Stop)	Output unit fuse blown.	(1) Check fuse blown indicator LED on output modules. (2) Examine special registers D9100 to D9107 to establish I/O location of blown fuse.
"CONTROL-BUS ERR." (Checked during execution of FROM and TO instructions)	40	Stop	Incorrect FROM and/or TO instruction execution. (1) Special function unit control bus error.	(1) Hardware fault (CPU, special function unit and/or base unit). Consult Mitsubishi representative.
"SP. UNIT DOWN" (Checked during execution of FROM and TO instructions)	41	Stop	No response from special function unit after execution of FROM and/or TO instruction. (1) Possible hardware fault.	Consult Mitsubishi representative.
"LINK UNIT ERROR" (Checked at power-on, STOP → RUN and PAUSE → RUN)	42	Stop	(1) AJ71R22 or AJ71P22 located in master station.	(1) Remove AJ71R22, AJ71P22 from master station (invalid configuration) and reset PC.
"I/O INT. ERROR" (Checked at the occurrence of interruption)	43	Stop	Interrupt signal received with no interrupt module present.	(1) Consult Mitsubishi representative.
"SP. UNIT LAY. ERR." (Checked at power-on, STOP → RUN and PAUSE → RUN)	44	Stop	(1) Three or more computer link units are installed in one CPU system. (2) Two or more AJ71P22 or AJ71R22 units are installed in one CPU system. (3) Two or more interrupt units are installed in one CPU system. (4) Parameter I/O allocation is incompatible with actual I/O system.	(1), (2), (3) Correct system configuration. (4) Correct parameter I/O allocation.
"SP. UNIT ERROR" (Checked during execution of FROM and TO instructions)	46	Stop (Run)	(1) No special function unit in I/O slot addressed by FROM and/or TO instruction.	(1) Examine the program step indicated by the diagnostics and correct.

Table 7.1 Error Code List (Continued)

Error Message	Content of Special Register D9008 (BIN value)	Resulting CPU Status	Error and Cause	Corrective Action
"LINK PARA. ERROR" (Checked at power-on, STOP → RUN and PAUSE → RUN)	47	Run	(1) Invalid or incompatible link parameters (may be caused by noise). (2) 0 slave stations set.	(1) Re-write link parameters from peripheral programming unit to PC. (2) Persistent error occurrence may indicate hardware fault. Consult Mitsubishi representative.
"OPERATION ERROR" (Checked during execution of instruction)	50	Run (Stop)	(1) The result of BCD conversion has exceeded the specified range (9999 or 9999 9999). (2) Operation impossible because specified device range has been exceeded. (3) File registers used in program without parameter setting.	(1) Examine the program step indicated by the PC diagnostics and correct.
"MAIN CPU DOWN" (Interrupt fault)	60	Stop	(1) INT instruction processed in microcomputer program area. (2) CPU malfunction due to noise. (3) Hardware fault.	(1) Remove INT. (2) Eliminate noise. (3) Consult Mitsubishi representative.
"BATTERY ERROR" (Checked at power-on)	70	Run	(1) Battery voltage low. (2) Battery not connected.	Connect battery for RAM and/or power failure data back up.

Table 7.1 Error Code List (Continued)

7.4 I/O Connection Troubleshooting

7.4.1 Input wiring troubleshooting

This section describes possible problems with the input circuit and corrective actions.

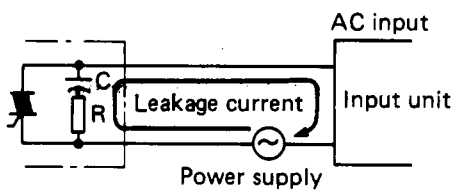
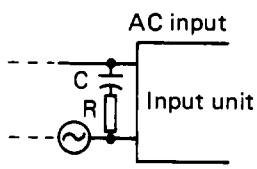
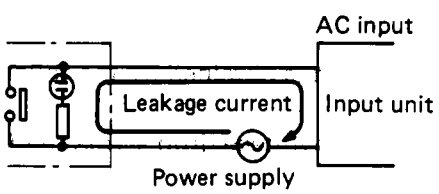
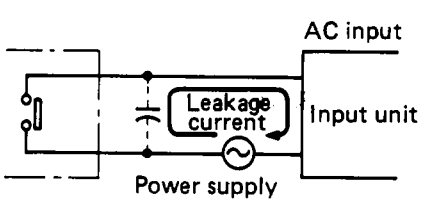
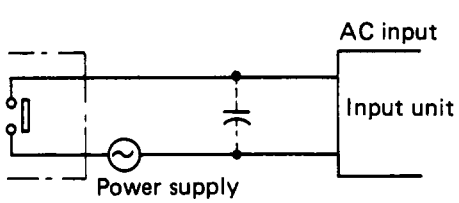
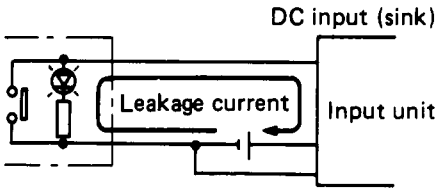
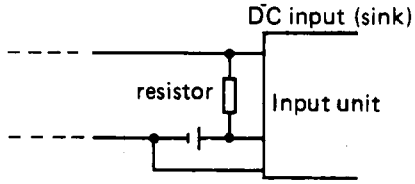
	Condition	Cause	Corrective Action
Example 1	AC input signal does not turn off. (Input LED may remain on or flicker)	• Input device leakage current. 	• Connect a CR network across input to drop the voltage below the input modules OFF threshold.  Use C = 0.1 to 0.47μF and R = 47 to 120Ω (1/2W)
Example 2	AC input signal does not turn off. (Input LED may remain on or flicker)	• Leakage current due to contact switch with neon indicator. 	• As example 1, or. • Construct independent indicator circuit.
Example 3	AC input signal does not turn off. (Input LED may remain on or flicker)	• Leakage current due to line capacity of wiring cable. (Line capacity of twisted pair wire is approx. 100 PF/m.) 	• As example 1. • Note that moving the power supply to the input device end of the cable will prevent leakage current from being generated. 
Example 4	DC input signal does not turn off. (Input LED may remain on or flicker)	• Leakage current due to contact switch with LED indicator. 	• Connect a resistor across the input and COM to drop the voltage below the input modules OFF threshold.  • Sample resistor value calculation given on next page.

Table 7.2 Input Wiring Troubleshooting

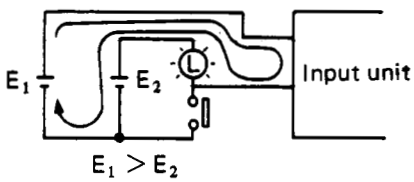
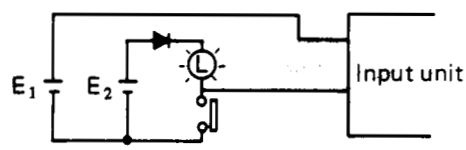
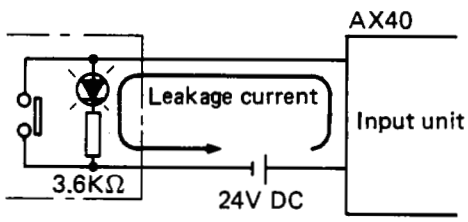
	Condition	Cause	Corrective Action
Example 5	DC input signal does not turn off. (Input LED may remain on or flicker)	• Current flow due to the use of two power supplies. 	• Use single power supply. • Use diode as shown below: 

Table 7.2 Input Wiring Troubleshooting (Continued)

Example:

Calculation for Example 4

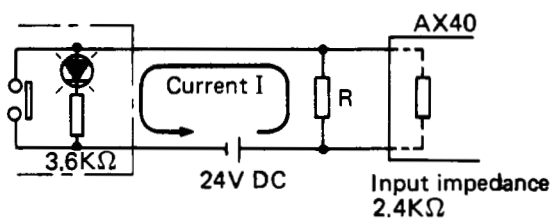


Consider a contact switch with LED indicator connected to an AX40 module, giving a 4mA leakage current.

- The voltage V_{TB} across terminal and common is obtained by the following expression:

  $V_{TB} = 4[mA] \times 2.4[K\Omega] = 9.6[V]$ (The voltage drop across the LED may be ignored.)

  The OFF threshold voltage is 6V so that the input will remain energized when the contact switch is open. Use resistor R as shown below:



- Calculate the resistor value, R, as shown below:
  For an input voltage < 6V, current I must be:

  $(24 - 6[V]) \div 3.6[K\Omega] = 5mA$

  Resistor R must be selected to give a current I > 5mA.

- Hence, for resistor, R

  $6[V] \div R > 5 - 2.5[mA]$
  $6[V] \div 2.5[mA] > R$
  $2.4[K\Omega] > R$

For R = 2KΩ, the power capacity must be:

W = (applied voltage)^2 /R (or W = (maximum current)^2 x R)

Resistor R terminal voltage is:

$$\frac{2.4 \times 2}{2.4 + 2}(K\Omega) : \frac{2.4 \times 2}{2.4 + 2} + 3.6(K\Omega) = X : 24(V)$$

$$X = 5.58(V)$$

Therefore, the power capacity W of resistor R is

$$W = (5.58[V])^2/2[K\Omega] = 0.015[W]$$

- Use a safety factor of 3 to 5. Resistor should therefore be rated at 0.5 to 1W.

  A 3kΩ, 0.5 to 1W resistor should therefore be connected across the relevant input terminal and its COM.

7.4.2 Output wiring troubleshooting

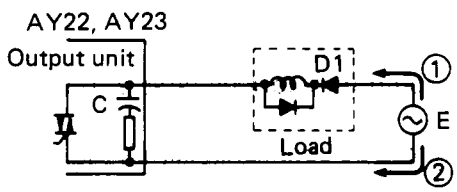
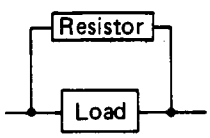
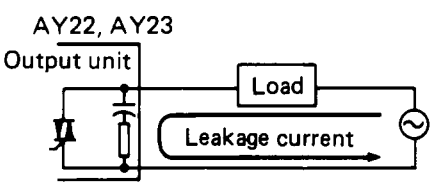
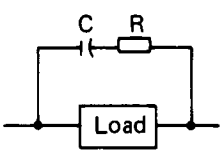
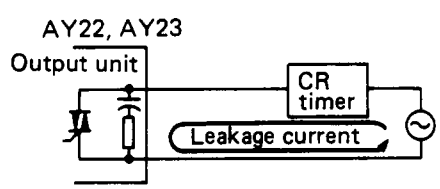
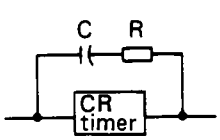
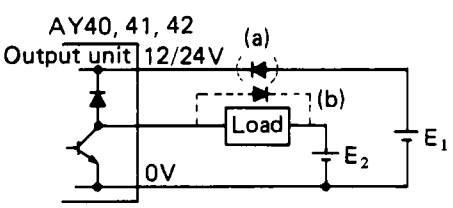
	Condition	Cause	Corrective Action
Example 1	AC voltage applied to output load when output in off.	• Half vave rectification by load (typical of some solenids).  • Current flow in direction ① causes capacitor, C, to charge. Current flow in direction ② applies capacitor voltage plus E across D1 (Voltage = 2.2E (approx)).	• Connect a resistor of several ten KΩ to several hundred KΩ across the load. Note: This solution may lead to damage to the diode. Suitable output loads should be substituted for the existing solenoids. 
Example 2	AC load does not turn off.	• Leakage current due to built-in noise suppression. 	• Connect a CR network across the load. Where long cable runs between output module and load are used, there may be a leakage current due to the line capacity.  Use C = 0.1 to 0.47μF and R = 47 to 120Ω.
Example 3	AC load is C-R type timer, time constant fluctuates.		• Drive the CR type timer from the same contact as the relay. Some timers have half-wave rectified internal circuits. Take precautions as indicated below:  CR values will depend on the load.
Example 4	DC load does not turn off.	• Current flow due to the use of two power supplies.  • When E1 < E2, current flows.	• Use single power supply. • Use diode (a) as shown on the left. When a relay (or similar load) is used, a free wheel diode should be connected across the load (see diode (b) on the left).

Table 7.3 Output Wiring Troubleshooting

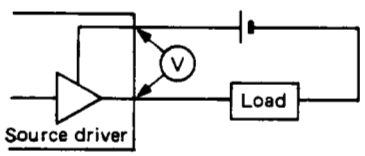
	Condition	Cause	Corrective Action
Example 5	Load does not operate normally (due to external shorting, etc.) AY60EP, AY80EP, AY81EP, AY82EP,	External load malfunction or incorrect connection.	● Check the external load. ● Check voltage across the following terminals with output (Y) on. ● If output voltage > 3V, check external load and wiring for short circuits. 

Table 7.3 Output Wiring Troubleshooting

POINT

Specifications for the RC network described in examples 2 and 4 are as follows:–

1) **Combination of C and R**

C	0.1μF	0.47μF	0.5μF
R	120Ω	47Ω	50Ω

2) **C may be a paper capacitor or metalized paper capacitor.**

3) **Capacitor voltage rating is 630V DC or 200V AC.**

4) **Resistor rating is 1/2W or more.**

5) **As a guide, for output load power consumption of 30VA use C = 0.47μF and R = 47Ω (approx.).**

8. MAINTENANCE AND INSPECTION

8.1 Daily Inspection

Number	Item		Check Point
1	Base unit mounting		Check for, and correct loose base unit mounting screws.
2	I/O module, special function unit, etc. mounting		Check that the units are securely engaged.
3	Connecting conditions		Check, and tighten, loose terminal screws.
			Check for, and correct, potential short circuits between solderless terminals.
			Check that extension cables are securely connected.
4	Main unit indicator LEDs	"POWER" LED	Check that the LED is on.
		"RUN" LED	Check power LED. If off refer to sect. 7.2.3, 7.2.4.
		Input LED	Check that input LEDs are functioning when input device switches on. If not, refer to sect. 7.2.5.
		Output LED	Check that output LEDs are functioning when driven from program. If not, refer to section 7.2.5.

Table 8.1 Daily Inspection

8.2 Six to Twelve Monthly Inspection

Number	Item		Check Point
1	Ambient environment	Ambient temperature	All environmental conditions inside the PC's enclosure should meet the specifications given in Section 3.1.
		Ambient humidity	
		Ambience	
2	Line voltage		Should be within the ranges specified in Section 3.3.1.
3	General	Mounting	Check that all modules and units are secured and tighten mounting screws as appropriate.
		Contamination by dust, dirt etc.	Check for, and remove any dust, dirt etc. which may have gathered on the PC.
4	Terminations and connectors	Terminal screws	Check and retighten terminal screws.
		Clearance between solderless terminals	Check and space solderless terminals as necessary.
		Loose connectors	Check and retighten connector fastening screws.
5	Battery		Check battery status by monitoring special auxiliary relays M9006 and M9007. Replace battery if necessary.
6	Fuse		Check fuses. Periodic fuse replacement is recommended as preventive maintenance.

Table 8.2 Periodic Inspection

8.3 Replacement of Battery

Special auxillary relays M9006 and M9007 are switched on to indicate that the battery life has reduced to approx. 168 hours (minimum) and that it must be replaced if continued power failure RAM and/or data back-up is required.

8.3.1 Battery service life

The battery life varies with memory size as shown below:

CPUtype, memory cassette type / Battery Life	Battery Life (Total power failure time) [Hr]	
	Guaranteed (minimum)	Actual (Average)
A3MCA- 0	10800	27000
A3MCA- 2	7200	18000
A3MCA- 4	5400	13000
A3MCA- 8	3600	9000
A3MCA-12	2150	5400
A3MCA-18	1950	4900

Table 8.3 Battery Life

The following additional preventive maintenance should be observed:

1) Replace any battery after 4 to 5 years.

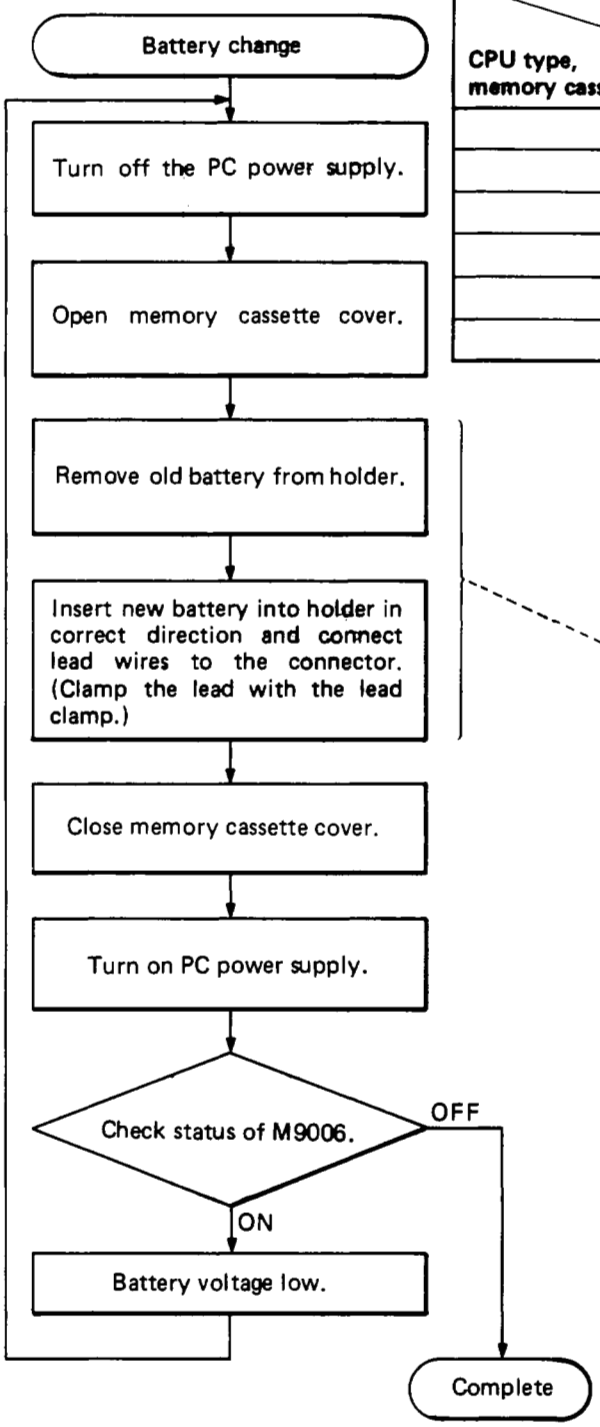
2) Replace any battery which has given power failure back up for the guaranteed period or longer, even if M9006, M9007 have not switched on.

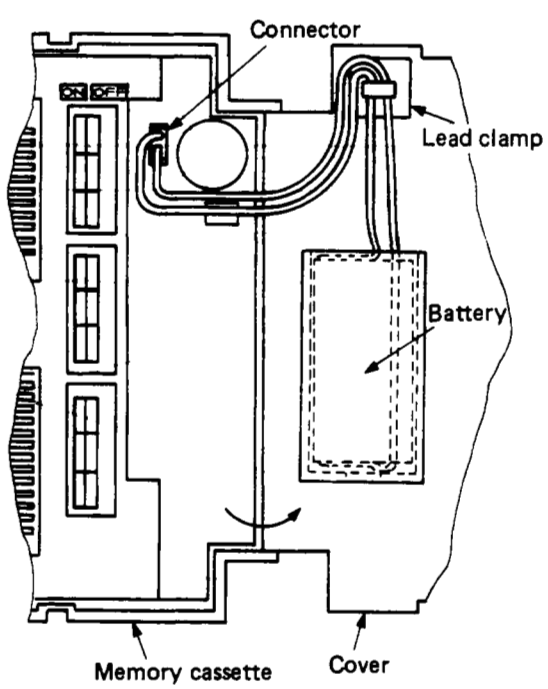
8.3.2 Changing the battery

Memory back up during battery replacement is provided by a capacitor. The back up time varies with memory size as shown in the table below:

Battery Life / CPU type, memory cassette type	Capacitor Backup Time [Minute]	
	Guaranteed (minimum)	Actual (Average)
A3MCA-0	18	45
A3MCA-2	12	30
A3MCA-4	9	20
A3MCA-8	6	15
A3MCA-12	4	10
A3MCA-18	3	8

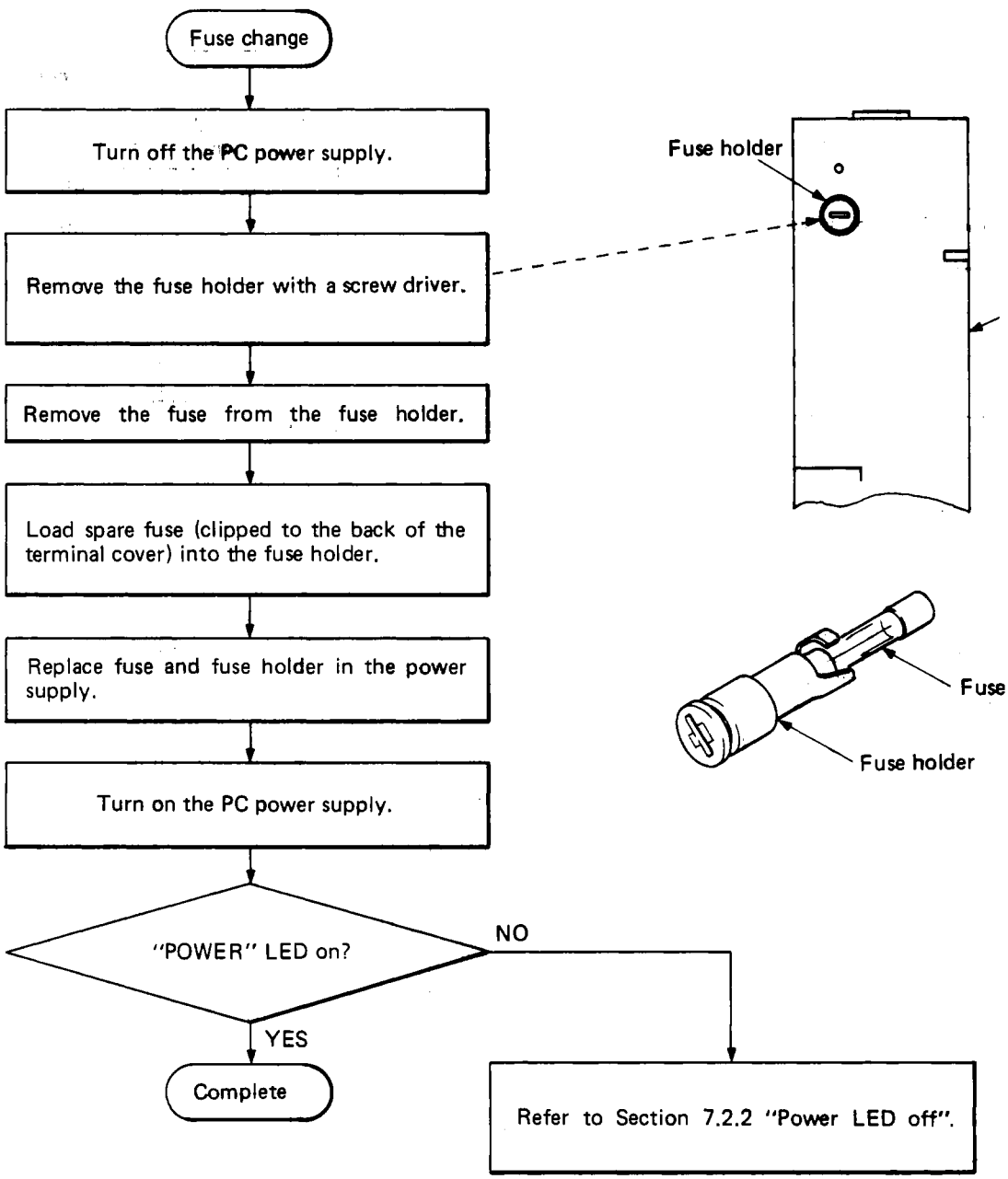
Table 8.4 Capacitor Back up Time


Battery change
Turn off the PC power supply.
Open memory cassette cover.
Remove old battery from holder.
Insert new battery into holder in correct direction and connect lead wires to the connector. (Clamp the lead with the lead clamp.)
Close memory cassette cover.
Turn on PC power supply.
Check status of M9006.
OFF
ON
Battery voltage low.
Complete

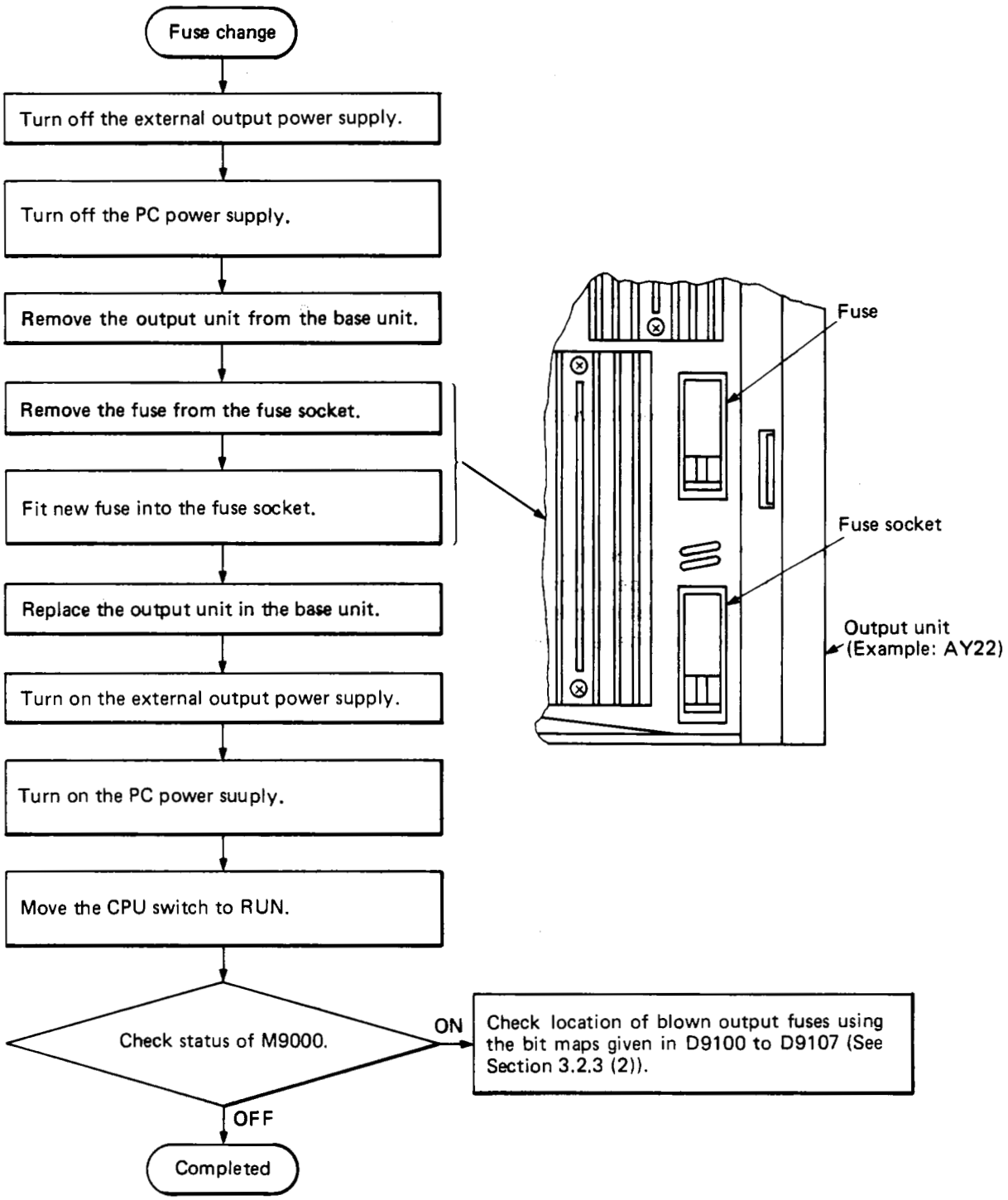


8.4 Fuse Replacement

8.4.1 Power supply fuse replacement


Fuse change
Turn off the PC power supply.
Remove the fuse holder with a screw driver.
Remove the fuse from the fuse holder.
Load spare fuse (clipped to the back of the terminal cover) into the fuse holder.
Replace fuse and fuse holder in the power supply.
Turn on the PC power supply.
"POWER" LED on?
NO
YES
Complete
Refer to Section 7.2.2 "Power LED off".
Fuse holder
Power supply unit
Fuse
Fuse holder

8.4.2 Output module fuse replacement


Fuse change
Turn off the external output power supply.
Turn off the PC power supply.
Remove the output unit from the base unit.
Remove the fuse from the fuse socket.
Fit new fuse into the fuse socket.
Replace the output unit in the base unit.
Turn on the external output power supply.
Turn on the PC power suuply.
Move the CPU switch to RUN.
Check status of M9000.
ON
Check location of blown output fuses using the bit maps given in D9100 to D9107 (See Section 3.2.3 (2)).
OFF
Completed
Fuse
Fuse socket
Output unit
(Example: AY22)

APPENDICES

APPENDIX 1 Differences in Instruction Set between A3HCPU and A1(E), A2(E), A3(E)CPU

The following instructions differ between the A3HCPU and the A1, A2, A3CPUs:

- PR instruction
- CHG instruction
- SEG instruction
- Subset processing condition
- Subset processable instructions

Other instructions are as described in the A1, A2, A3CPU Programming Manual.

1.1 Subset processing

Data transactions may be made between combinations of bit and word devices. For example, the notation:

BIN	K4X0	D0

will convert the BCD bit pattern on the 16 inputs X0 to XF to a binary bit pattern in D0.
The processing time for this type of data transaction partly depends on the starting point of the bit sequence. For optimum processing speeds, the bit sequence starting point should be 0 or a multiple of 16 (decimal). This is one of the requirements for "subset processing".

Examples:

BCD	D10	K4Y60	Processed as subset (Outputs numbered in Hex)
MOV	K4M0	K4M64	Processed as subset (Ms numbered in Dec)
BIN	K4B3	K4M16	Not processed as subset (B3 not a multiple of 16)

The following table specifies all the conditions necessary for subset processing:

		A3HCPU	A1, A2, A3CPU
Index qualification (i.e. use of V or Z)		Not used	Not used
Bit device	Digit specification	16-bit instruction . . . . . K4 32-bit instruction K8	16-bit instruction . . . . . K4 32-bit instruction K8
	Device number	A multiple of 16	A multiple of 8
Device		Devices other than file register (R) may be used.	All devices may be used.

The A3HCPU's subset processable instructions are the same as those for the A1, A2, A3CPU with the addition of the instructions given below.
For the A1, A2, A3CPU subset processable instructions, see the A1, A2, A3CPU Programming Manual.

1) CJ
2) CALL
3) SUM
4) JMP
5) SCJ
6) FOR
7) B+ (B+ | Source | Destination)
8) B– (B– | Source | Destination)
9) DSFR
10) DSFL
11) SEG
12) DBCD
13) DBIN
14) B✳
15) B/
16) BMOV
17) FMOV

1.1.1 EI and DI instructions

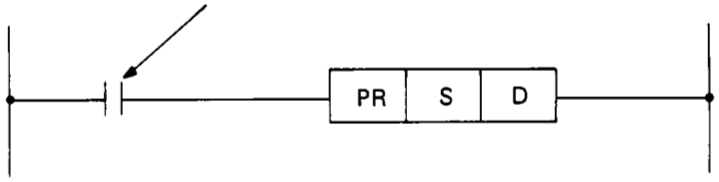
These instructions are used in the same way as for the A1E, A2E, A3ECPU when the A3HCPU has either or both its inputs and outputs in refresh mode. Note that the COM instruction must be enabled using the EI instruction if either or both the inputs and outputs are in refresh mode. For further information, refer to the A1(E), A2(E), A3(E)CPU programming manual.

1.2 PR instruction.....ASCII print

Processing Unit	Applicable CPU
—	A3H

	Usable Device																			Digit specification	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device						Word (16-bit) device									Constant		Pointer		Level					
	X	Y	M	L	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
S							○	○	○	○	○											7		○		
D		○																								○

ASCII print command



Set data

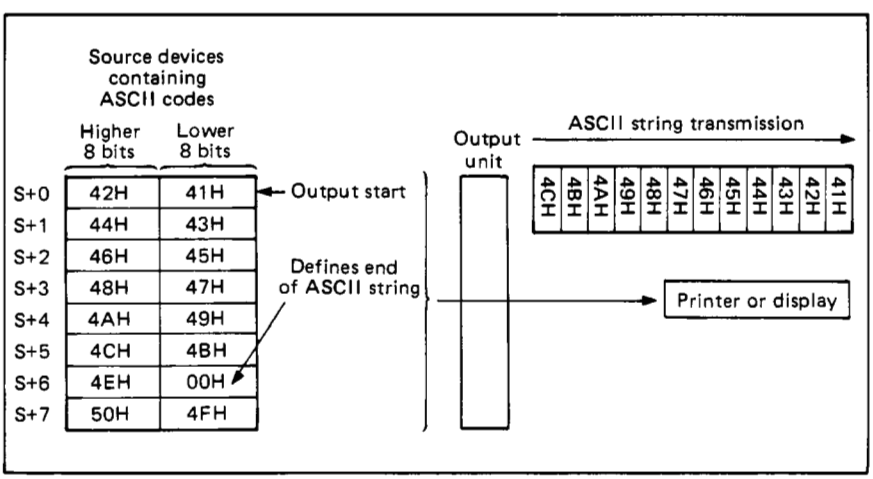
S	Head device of ASCII source data
D	Head output device destination for ASCII data.

POINT

There is no limit to the number of output characters for the A3HCPU PR instruction.

FUNCTIONS

(1) Transfers the ASCII code stored in the source devices to the group of 8 outputs specified by the head output device.



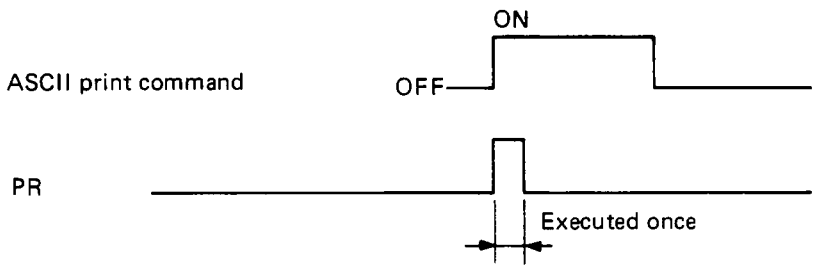
(2) Each character is transmitted in 30ms from the output unit, e.g. 480ms is required to transmit 16 characters (16 x 30ms). This is controlled independently of the PC scan time.

(3) In addition to the ASCII codes, a strobe signal (ON for 10ms, OFF for 20ms) is transmitted from the output unit.

(4) The PR instruction execution flag is switched on after the PR instruction is executed and remains on until all the specified ASCII codes are transmitted.

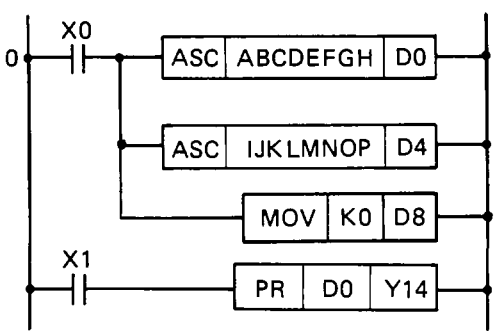
(5) If several PR instructions are used, the PR instruction execution flag must be used as an interlock to prevent them from being switched on simultaneously.

EXECUTION CONDITION



PROGRAM EXAMPLE

The following example converts "ABCDEFGHIJKLMNOP" into ASCII codes which are written to D0 to 7 when X0 is switched on and transmits the same codes to Y14 to 1D when X1 is switched on.



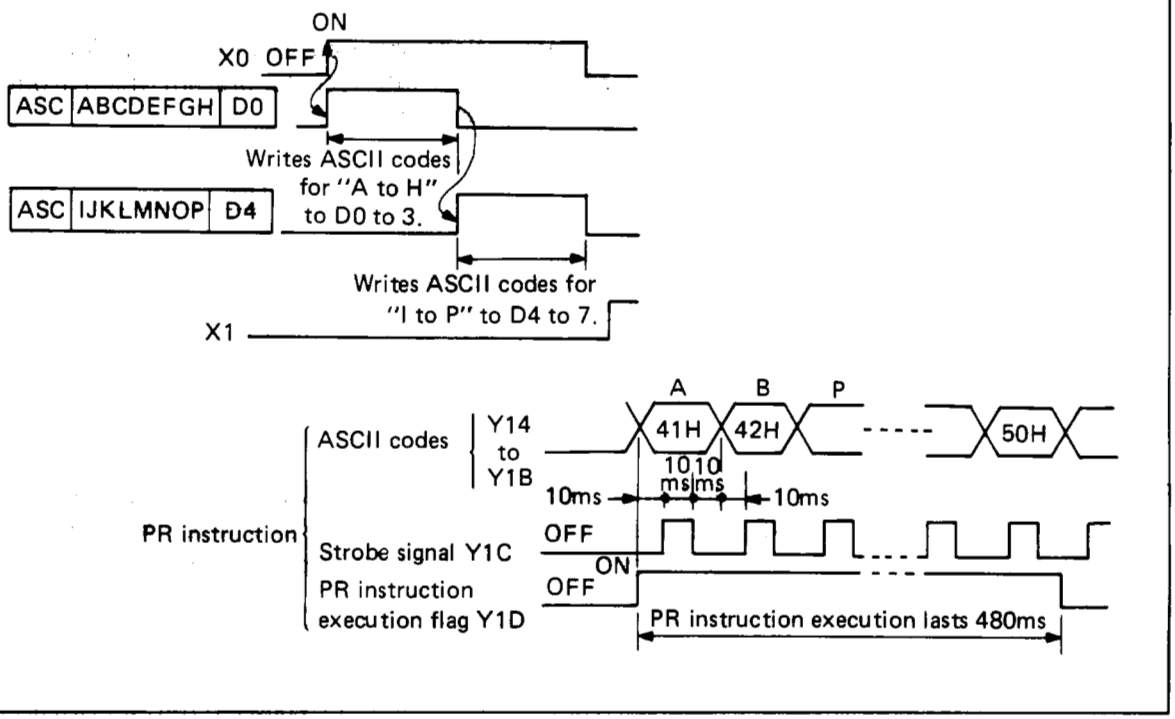
Converts "ABCDEFGHIJKLMNOP" into ASCII codes and writes to D0 to 7 when X0 is switched on.

Writes 00H code (specifying end of ASCII string) to D8.

Transmits the ASCII codes to Y14 to 1D when X1 is switched on.

Coding

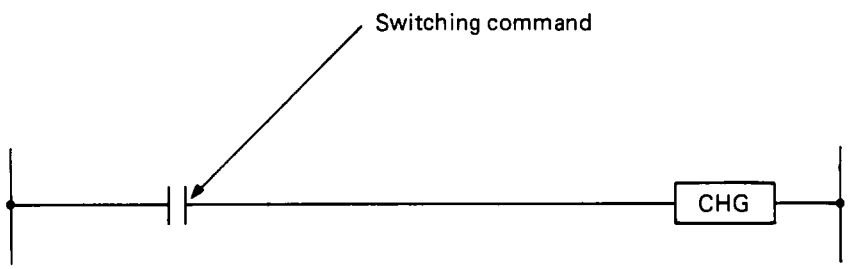
Step Number	Instruction	Device			
0	LD	X0			
1	ASC	ABCDEFGH	D0		
14	ASC	IJKLMNOP	D4		
27	MOV	K0	D8		
32	LD	X1			
33	PR	D0	Y14		
40	END				


ON
X0 OFF
ASC ABCDEFGH D0
Writes ASCII codes for "A to H" to D0 to 3.
ASC IJKLMNOP D4
Writes ASCII codes for "I to P" to D4 to 7.
X1
A
B
P
ASCII codes
Y14 to Y1B
41H
42H
50H
10ms
10ms
10ms
PR instruction
Strobe signal Y1C
OFF
ON
PR instruction execution flag Y1D
OFF
PR instruction execution lasts 480ms

1.3 CHG instruction.....Main/subprogram switching

Processing Unit	Applicable CPU
–	A3H

Usable Device																			Digit specification	Number of steps	Subset	Index	Carry flag	Error flag
Bit device						Word (16-bit) device									Constant		Pointer		Level					
X	Y	M	L	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
																					1				○

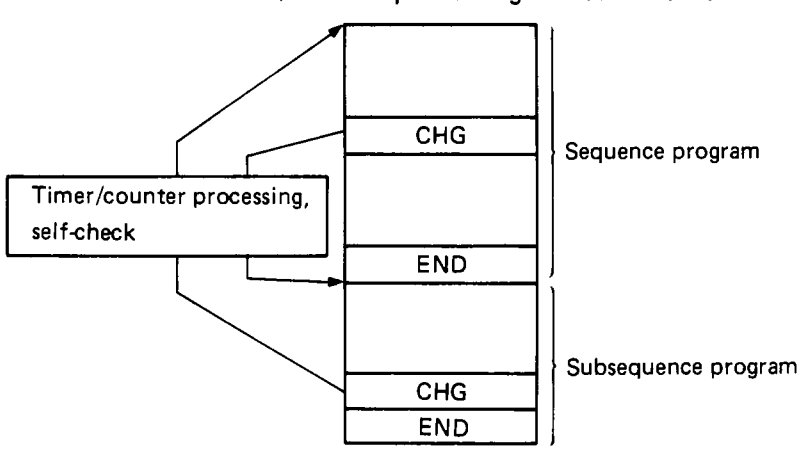


POINT

The CHG instruction is executed repeatedly while its switching command is on.

FUNCTIONS

(1) Switches the main program to the subprogram and vice versa after timer/counter processing and self-check.

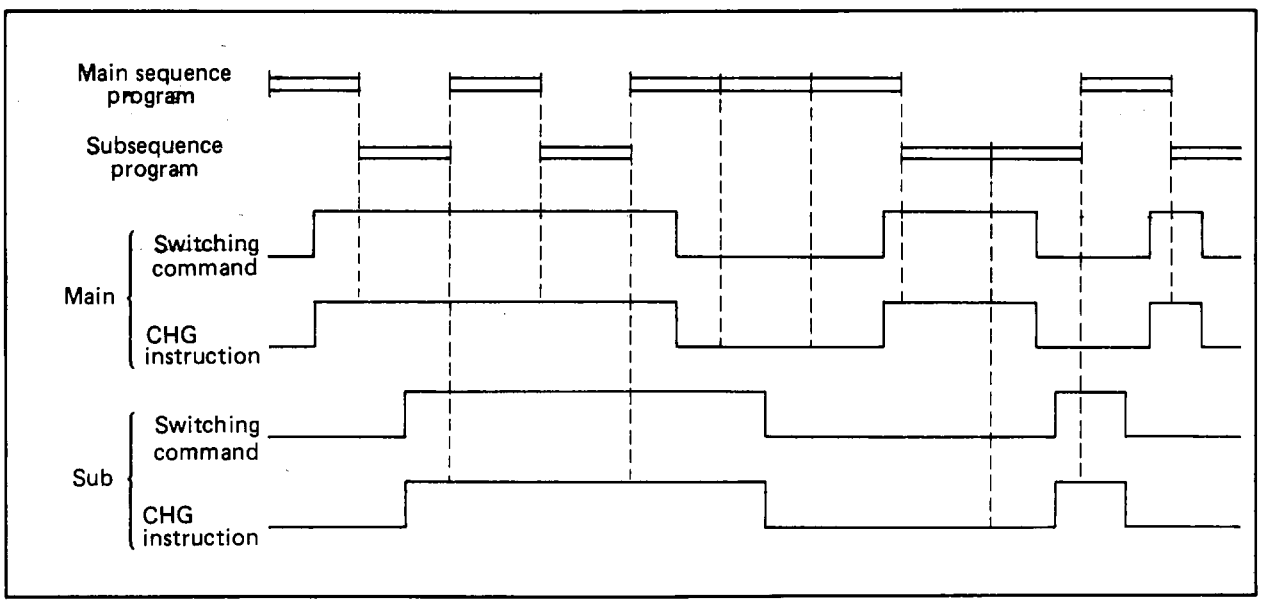


(2) Outputs are not switched off when the CHG instruction is executed. The program output data will therefore remain unchanged while the other program is being run.

(3) The CHG instruction may be enabled and disabled by special relay M9051 as described below:

With M9051 on, the CHG instruction is disabled.
With M9051 off, the CHG instruction is enabled.

EXECUTION CONDITION



1.4 SEG instruction

Application of this instructing differs depending on the state of special relay M9052 as described below:
Used as a partial refresh instruction if M9052 is on.
Used as a 7-segment display data decode instruction if M9052 is off.

This section describes the use of the SEG instruction as a partial refresh instruction. For the 7-segment display data decode instruction, refer to the A1(E), A2(E), A3(E)CPU Programming Manual.

POINT

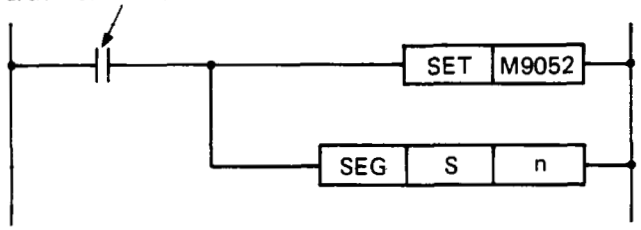
M9052 is switched on/off by the sequence program.

1.4.1 Partial refresh instruction

Processing Unit	Applicable CPU
–	A3H

	Usable Device																				Digit specification	Number of steps	Subset	Index	Carry flag	Error flag
	Bit device						Word (16-bit) device									Constant		Pointer		Level						
	X	Y	M	L	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9011
S	○	○																				7				○

Partial refresh command



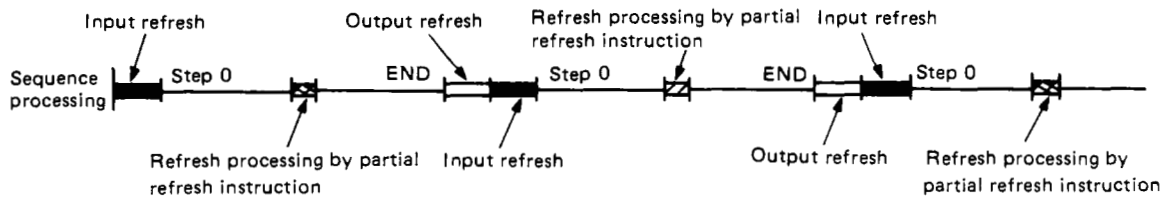
Set data

S	Head device number for refresh.
n	Number of points refreshed. Set in blocks of 8 points. (See (5).)

FUNCTIONS

(1) Refreshes the number of devices, n, beginning with device number, S.

(2) The partial refresh function refreshes the specified devices part way through a scan.



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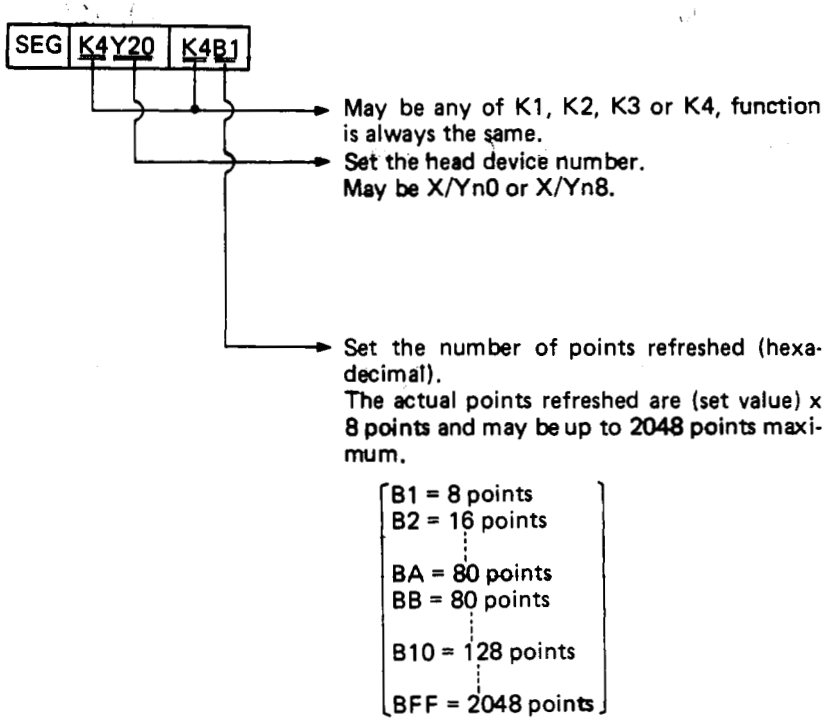
(3) The partial refresh instruction may be used to update rapidly changing input data more frequently.

(4) The status of an output device may be changed more than once during a scan by executing a partial refresh immediately after its coil has been used in the program.

(5) Data must be set to S and n as follows:


SEG
K4Y20
K4B1
May be any of K1, K2, K3 or K4, function is always the same.
Set the head device number.
May be X/Yn0 or X/Yn8.
Set the number of points refreshed (hexadecimal).
The actual points refreshed are (set value) x 8 points and may be up to 2048 points maximum.
B1 = 8 points
B2 = 16 points
BA = 80 points
BB = 80 points
B10 = 128 points
BFF = 2048 points

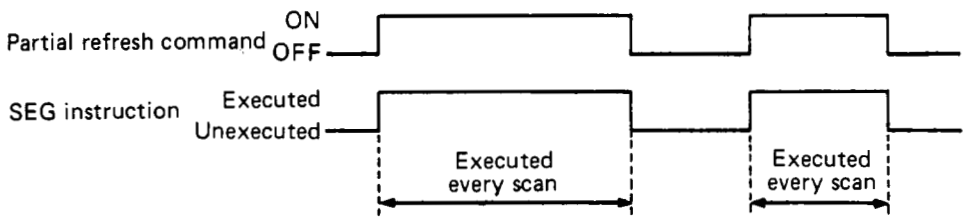
POINT

Setting B0 (0 point) refreshes all devices in the unit, beginning with the head device number specified.

POINT

Partial refresh processing is still performed if the SEG instruction is executed with the A3HCPU set in X/Y direct mode, but in this case, input (X)/output (Y) ON/OFF status does not change.

EXECUTION CONDITION



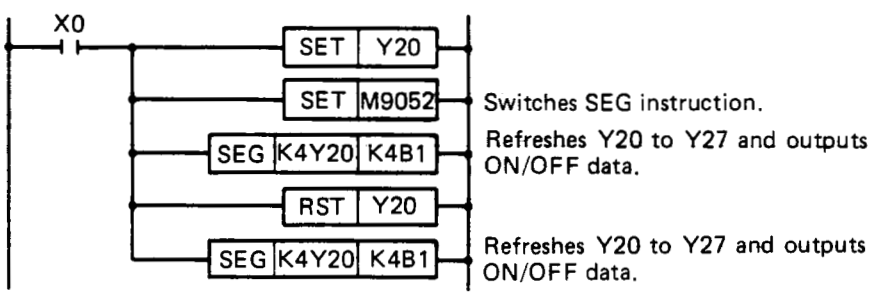
OPERATION ERROR

The error flag is switched on if:

- Any invalid data is set in S or n.
- The partial refresh range exceeds X, Y7FF.

PROGRAM EXAMPLE

The following example switches output Y20 on and off within one scan.



Coding

Step Number	Instruction	Device			
0	LD	X0			
1	SET	Y20			
2	SET	M9052			
5	SEG	K4Y20	K4B1		
11	RST	Y20			
13	SEG	K4Y20	K4B1		
19	END				

APPENDIX 2 Notes on Compatibity of the A3HCPU with the A1(E), A2(E), A3(E)CPUs

Note the following points regarding hardware and software compatibity between the A3HCPU and the A1(E), A2(E), A3(E)CPU.

2.1 Notes on use of the A3HCPU instead of the A1, A2, A3CPU

2.1.1 Power supply units

The main base unit current capacity must be checked since the A3HCPU consumes more current than the A1(E), A2(E), A3(E)CPU as shown below.

	A3HCPU	A1CPU	A2CPU	A3CPU
Current consumption (5V DC)	3.0A	1.5A	1.6A	1.7A

(Optical data link)

	A3HCPUP21	A1CPUP21	A2CPUP21	A3CPUP21
Current consumption (5V DC)	3.7A	3.4A	3.5A	3.6A

(Coaxial data link)

	A3HCPUR21	A1CPUR21	A2CPUR21	A3CPUR21
Current consumption (5V DC)	4.1A	3.7A	3.8A	3.9A

POINT

The A65P power supply unit cannot be used in the main base unit in an A3HCPU system.

2.1.2 Extension bases (A55B, A58B)

When using the A55B or A58B check that sufficient 5V DC capacity is available from the power supply unit on the main base unit.
See Section 3.4.3 for voltage drop along the extension cable when used with the A55B or A58B.

2.1.3 Special function units

The following restrictions apply to the use of certain special function units:

(1) AJ71C24.....Must be applicable to the A3HCPU. (See Section 2.2.1.)
(2) AD51 .....Must be applicable to the A3HCPU. (See Section 2.2.1.)
(3) AJ71C23.....Cannot be used.
(4) AD57 .....Cannot be used.
(5) AD58 .....Cannot be used.

2.1.4 Peripherals

The following restrictions apply to the use of peripheral equipment with the A3HCPU:

(1) A6GPP/PHP . . . . .Software package SW3GP-GPPA□□-1/2 or subsequent versions.
(2) A6HGP . . . . . .Software package SW3-HGPA□□-1/2 or subsequent versions.
(3) A7PU . . . . . .Must be applicable to the A3HCPU. (See Section 2.2.1.)
(4) A6WU . . . . . .Must be applicable to the A3HCPU. (See Section 2.2.1.)

2.2 Notes on use of the A1, A2, A3CPU sequence programs with the A3HCPU

Programs written for A1(E), A2(E), A3(E)CPU may be used in the A3HCPU with the following points corrected:

(1) Parameter setting
(2) I/O control mode switching
(3) Multiple output switching during one scan using SET/RST instructions (depends on output processing modes, direct or refresh).
(4) Data link processing
(5) Special relays, special data registers
(6) PR instruction
(7) CHG instruction
(8) Interrupt program
(9) Microcomputer program

2.2.1 Parameter setting

A1(E), A2(E), A3(E)CPU programs can be used without changing parameter setting. In this case, the additional parameters and watch dog timer for the A3HCPU are automatically set as follows:

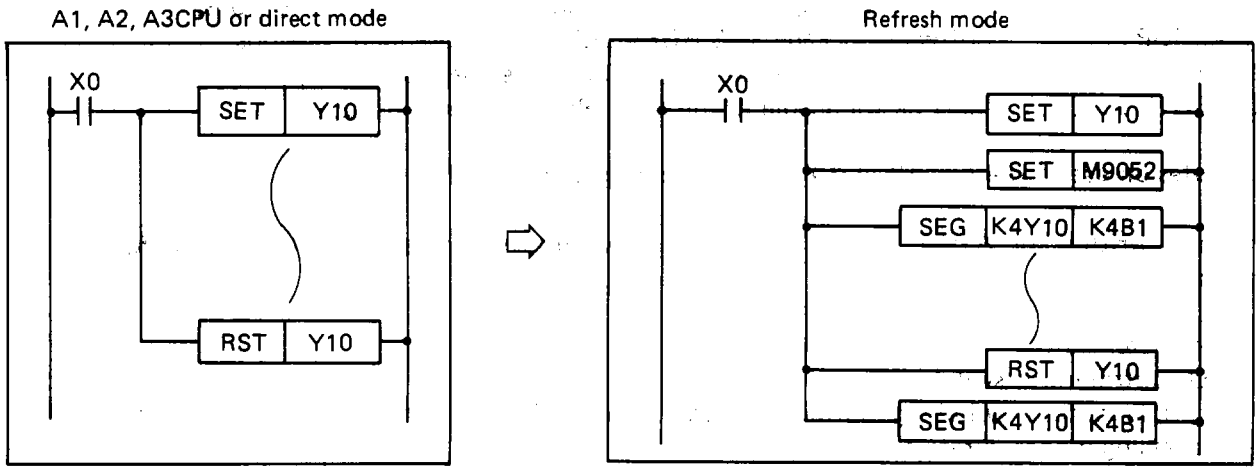
(1) Watch dog timer . . . . . .200ms irrespective of the set value.
(2) I/O control mode . . . . . .Both input and output in direct mode
(3) Interrupt counter . . . . . .None

2.2.2 I/O control mode switching

The A3HCPU allows input (X) and output (Y) control to be switched to direct or refresh mode. Processing is the same as in the A1, A2, A3CPU if direct mode is selected for both input and output.
Input and output timings are different if refresh mode is selected. For further details, see Section 3.2.9.

2.2.3 Multiple switching of a given output within one scan

The partial refresh instruction must be used as shown below to output pulse signals using the SET/RST instructions with the A3HCPU output (Y) in refresh mode.



POINT

This type of output processing is required when using the A3HCPU (output refresh mode) with the AD61 high speed counter.

2.2.4 Data link processing

Link refresh timing differs as follows. The program must be corrected if program execution is affected by the link refresh.

	A3HCPUP21/R21	A1, A2, A3CPUP21/R21
As master station	After END instruction	• After END instruction if program scan time is greater than link scan time. • After link scan or during program execution if program scan time is less than link scan time.
As local station	After END instruction	Interrupt from the master station (only once during one scan).

For details, see the A3HCPUP21/R21 Data Link Unit User's Manual.

2.2.5 Special relays, special data registers

The following special relays and special data registers are not used in the A3HCPU.

(1) M9010. . . . . .Flag indicating occurence of an operation error (Switched off when the error is removed.)

(2) M9050. . . . . .CHG instruction execution flag.

(3) D9010. . . . . .Stores the step number at which an operation error has occurred.

2.2.6 PR instruction

The specifications are different as follows:

	A3HCPU	A1, A2, A3CPU
Number of characters	As specified by user program	16 only

For details, see Appendix 1.2.

2.2.7 CHG instruction

The specifications are different as follows:

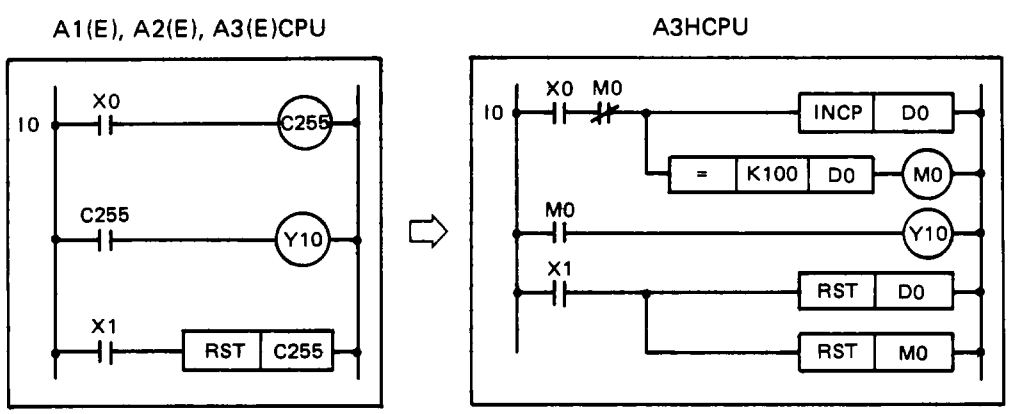
	A3HCPU	A3CPU
CHG instruction	Executed repeatedly while the condition contact is on	Executed on the leading edge of the condition contact

The A3HCPU contains two separate "operation result memory areas", one for the main and one for the subsequence program. These memory areas are used to store the contact statuses relevant to processing leading/trailing edge triggered instructions. The A3(E)CPU only has one "operation result memory area" which can be cleared by switching special relay M9050 on. The A3HCPU does not use the M9050 special relay.

2.2.8 Interrupt program

The A1(E), A2(E), A3(E)CPU type interrupt counters are not available for the A3HCPU. Data register must therefore be used as counters in A3HCPU interrupt programs.

Example



• Counter has been replaced by a data register (D0)

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2.2.9 Microcomputer program

(1) Utility packages

The following utility packages cannot be used with the A3HCPU:

1) SW0-AD57P
2) SW0-UTLP-PID
3) SW0-UTLP-FN0

(2) User-written microcomputer program

Microcomputer program instructions written for the A1(E), A2(E), A3(E)CPU can be used in the A3HCPU.
In this case, addresses must be changed if devices are switched on/off or data is transferred by the microcomputer program.
The A3HCPU device memory areas and configurations are shown below.
For the A1(E), A2(E), A3(E)CPU device memory areas, see the A1(E), A2(E), A3(E)CPU Programming Manual.

Device	Address		Configuration
Input (X)	8000H to 80FFH	X0 to 7FF	Odd addresses / Even addresses B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 8000H XF XE XD XC XB XA X9 X8 X7 X6 X5 X4 X3 X2 X1 X0 8002H X1F X1E X1D X1C X1B X1A X19 X18 X17 X16 X15 X14 X13 X12 X11 X10 8004H X2F X2E X2D X2C X2B X2A X29 X28 X27 X26 X25 X24 X23 X22 X21 X20 ⇩ • Stores ON/OFF data from an input unit, read only. • 0 indicates ON and 1 OFF.
Output (Y)	8200H to 82FFH	Y0 to 7FF	Odd address / Even addresses B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 8200H YF YE YD YC YB YA Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 8202H Y1F Y1E Y1D Y1C Y1B Y1A Y19 Y18 Y17 Y16 Y15 Y14 Y13 Y12 Y11 Y10 8204H Y2F Y2E Y2D Y2C Y2B Y2A Y29 Y28 Y27 Y26 Y25 Y24 Y23 Y22 Y21 Y20 ⇩ • Stores ON/OFF data from an output unit, read only. • 0 indicates ON and 1 OFF. The output memory is accessed as shown below: Write → Output unit Read ← Output memory

Device	Address		Configuration
Internal relay (M) Latch relay (L) Step relay (S)	8400H to 84FFH	M/L0 to 2047	
Link relay (B)	8600H to 867FH	B0 to 3FF	
Annuciator (F)	8700H to 871FH	F0 to 255	
Special relay (M)	8740H to 875FH	M9000 to 9255	
Timer (T) contact	8780H to 879FH	T0 to 255	
Counter (C) contact	87C0H to 87DFH	C0 to 255	
Timer (T) coil	9C00H to 9C1FH	T0 to 255	
Counter (C) coil	9C40H to 9C5FH	C0 to 255	

- Stores device ON/OFF data in one bit locations.
- 0 indicates OFF and 1 ON.

Example: M0 to 47 are as follows:

	Odd area								Even area							
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
8400H	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
8402H	M31	M30	M29	M28	M27	M26	M25	M24	M23	M22	M21	M20	M19	M18	M17	M16
8404H	M47	M46	M45	M44	M43	M42	M41	M40	M39	M38	M37	M36	M35	M34	M33	M32

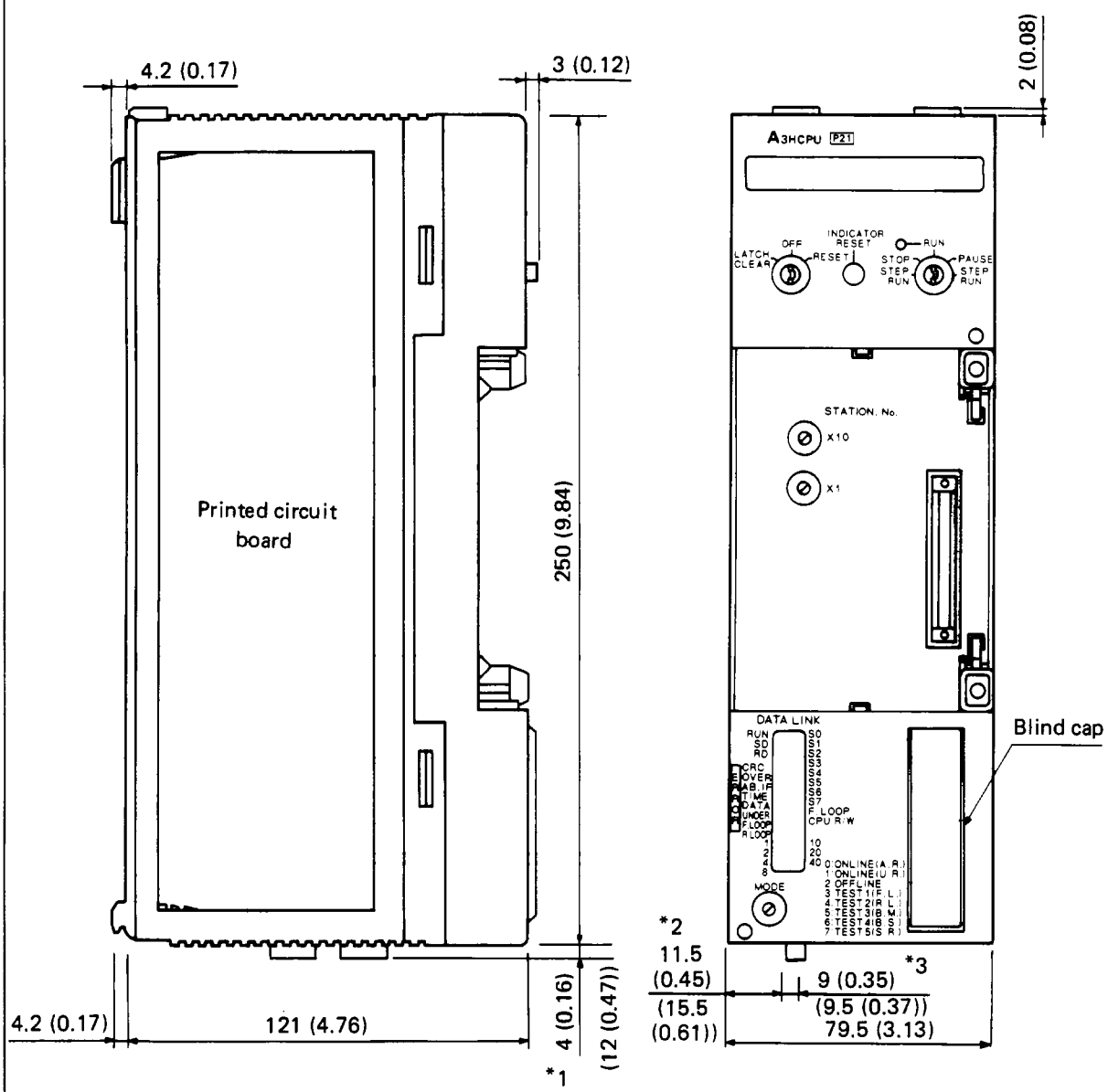
⇩

Stores PC operation results and allows read/write.

Device	Address	Configuration
Data register (D)	8800H to 8FFFH — D0 to 1023	All devices are in 2 byte (16 bit) locations. Example: D0 configuration is as follows: B7 … B0 / 8800H (L) / 8801H (H) / B15 … B8
Link register (W)	9000H to 97FFH — W0 to 3FF	
Timer (T) present value	9800H to 99FFH — T0 to 255	
Counter (C) present value	9800H to 9BFFH — C0 to 255	
Special register (D)	9D00H to 9EFFH — D9000 to 9255	
Accumulator (A0, 1)	9FF8H — A0 9FFAH — A1	
Index (Z, V)	9FFC — Z 9FFE — V	

APPENDIX 3 Dimensions

3.1 CPU unit

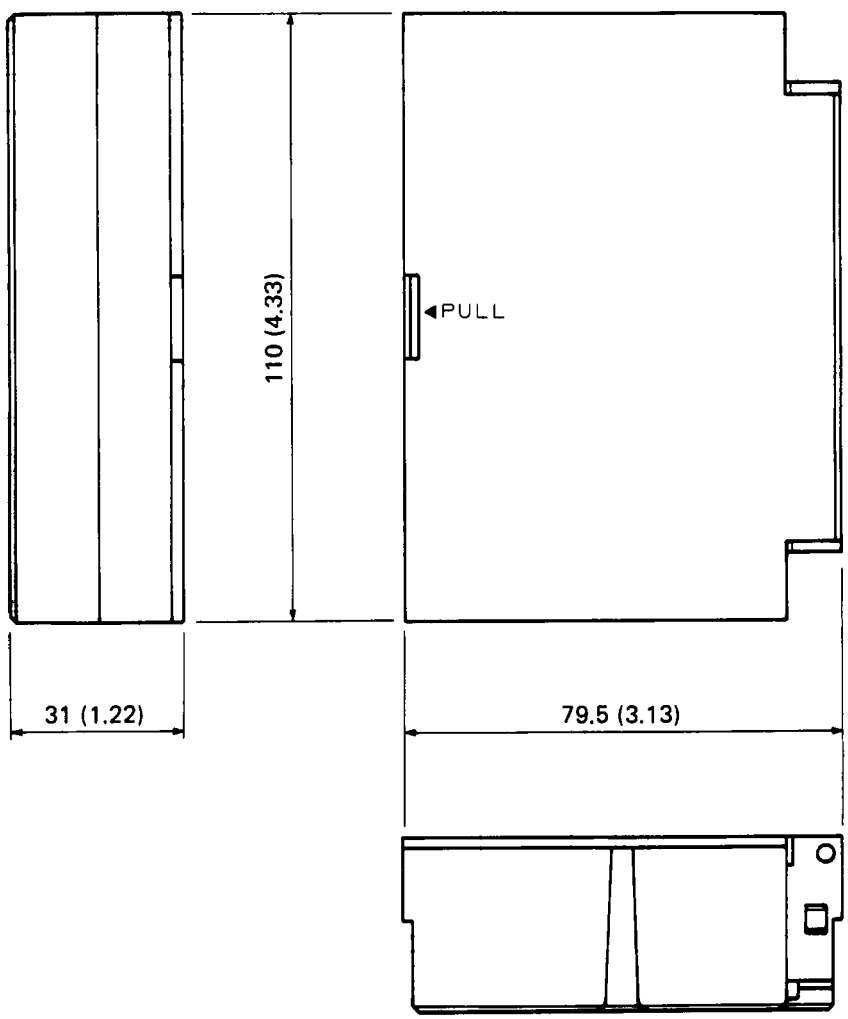


Unit: mm (inch)

REMARKS

Dimensions marked *1 to *3 are for the A3HCPUP21, those outside parentheses for the A3HCPUR21, and should be ignored for the A3HCPU.

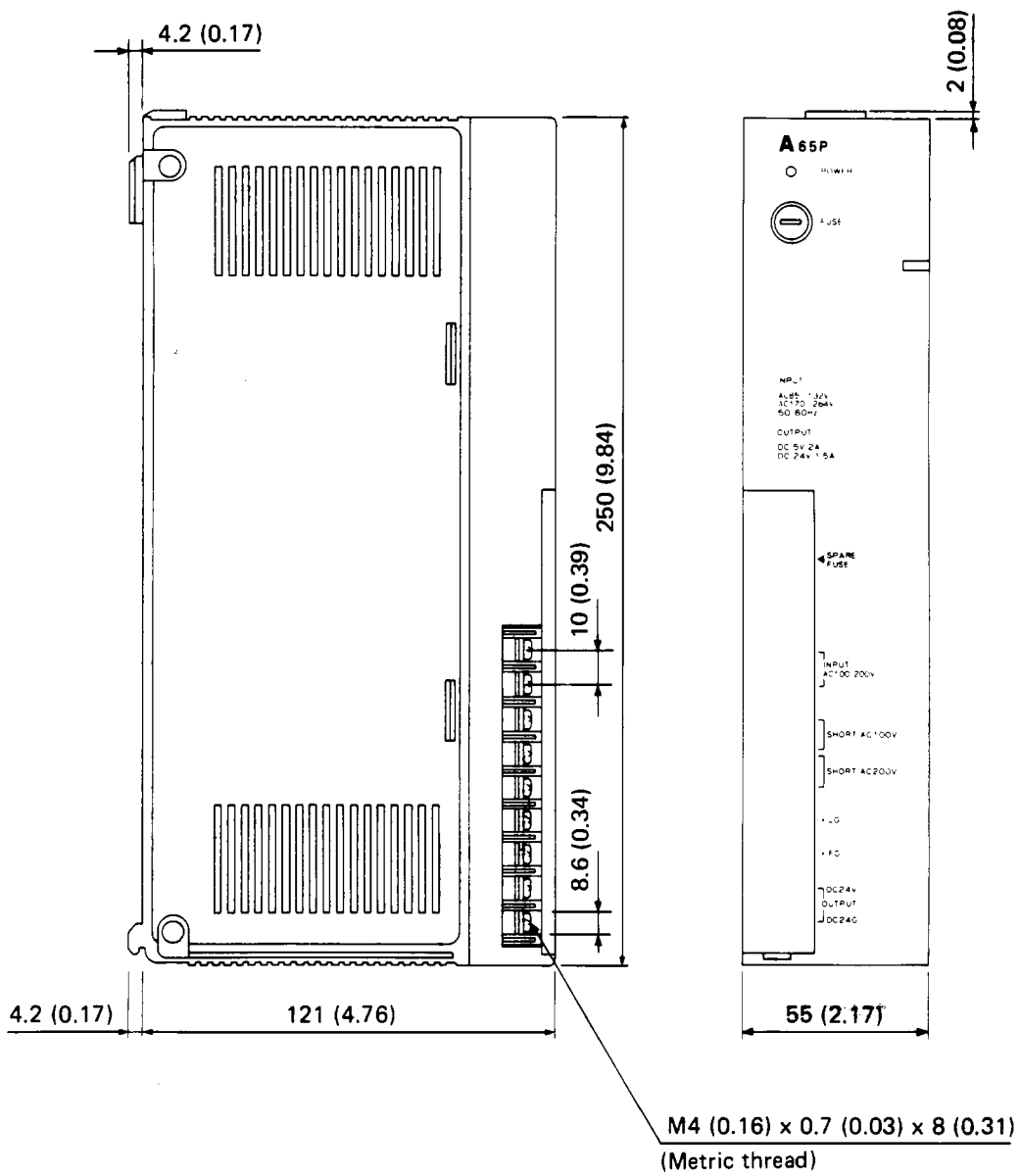
3.2 Memory cassettes (A3MCA-□)



Unit: mm (inch)

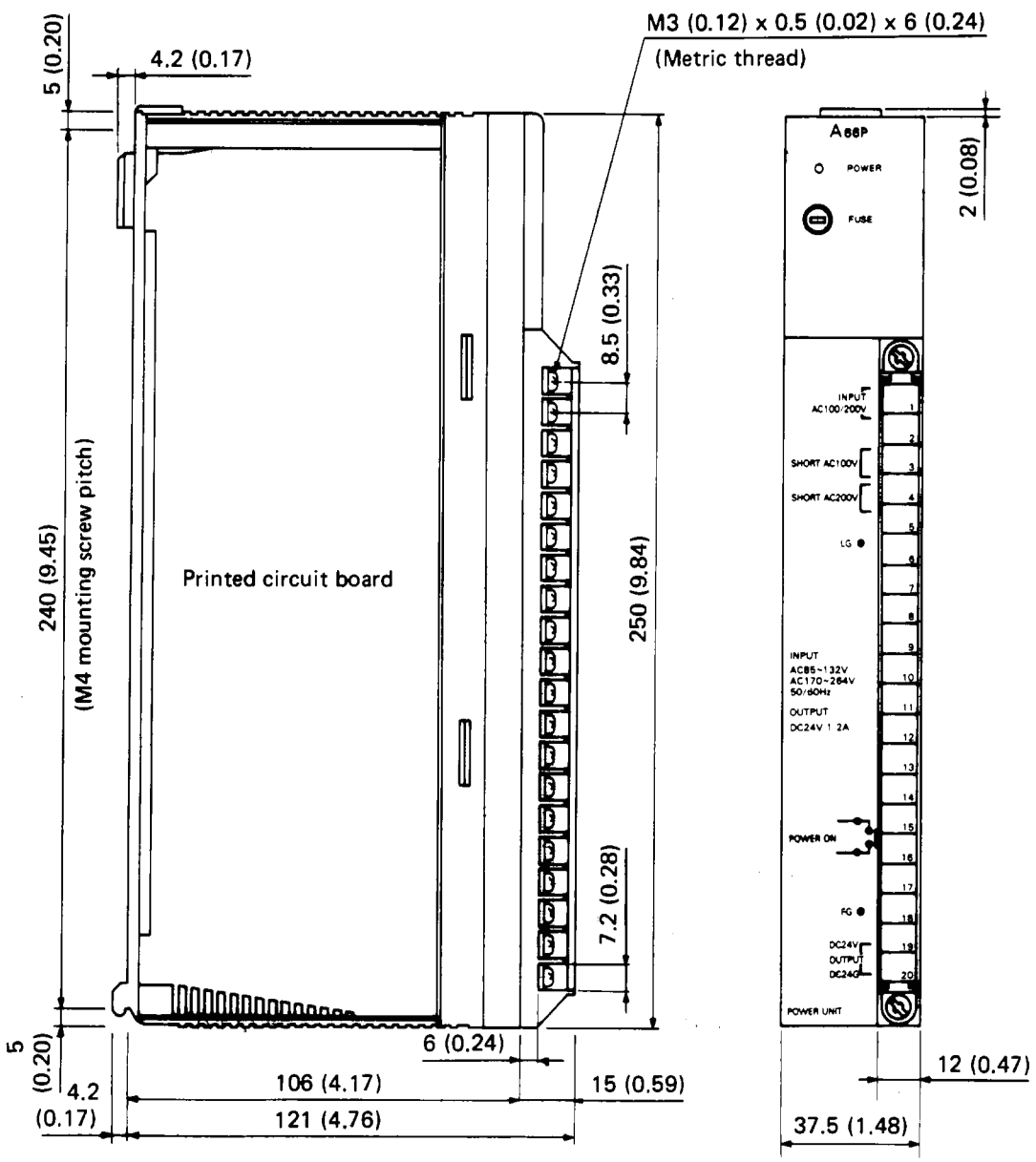
3.3 Power supply units

(1) Type A61P, A62P, A63P, A65P power supply units



Unit: mm (inch)

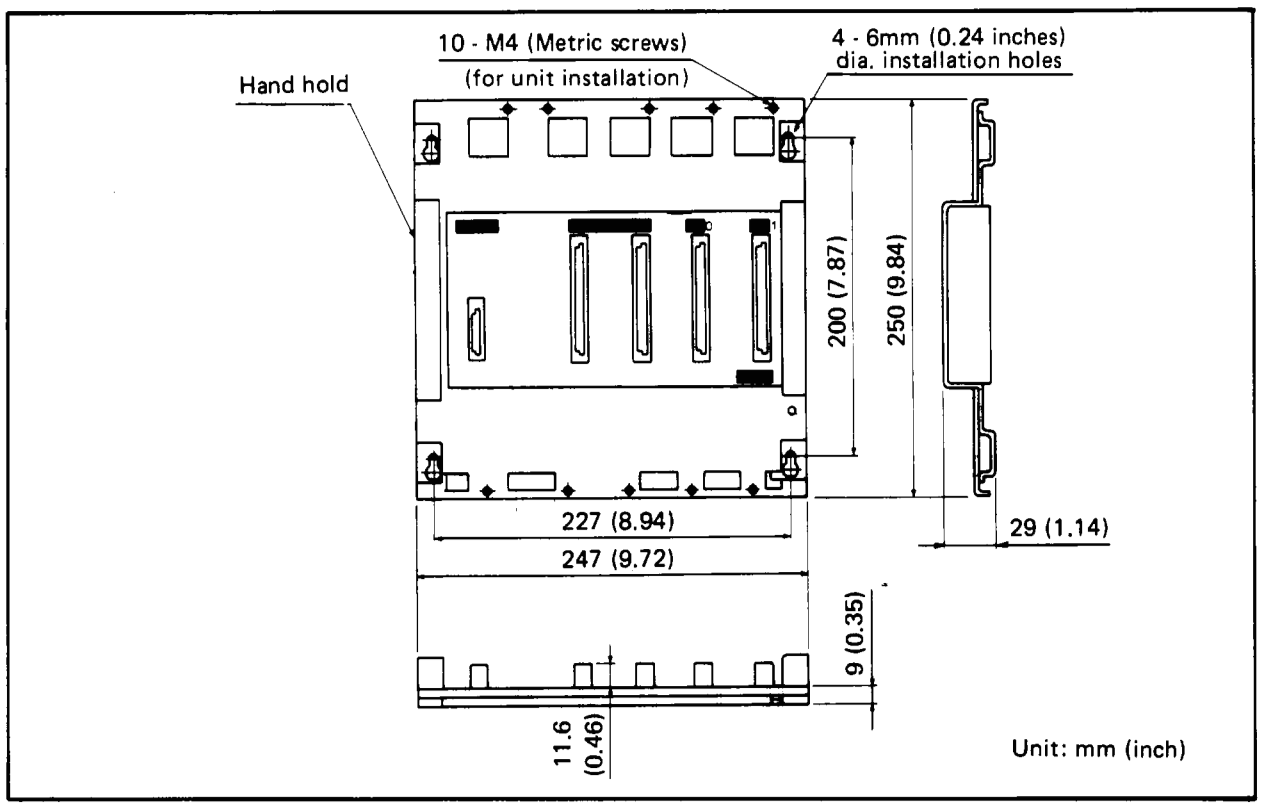
(2) Type A66P power supply unit



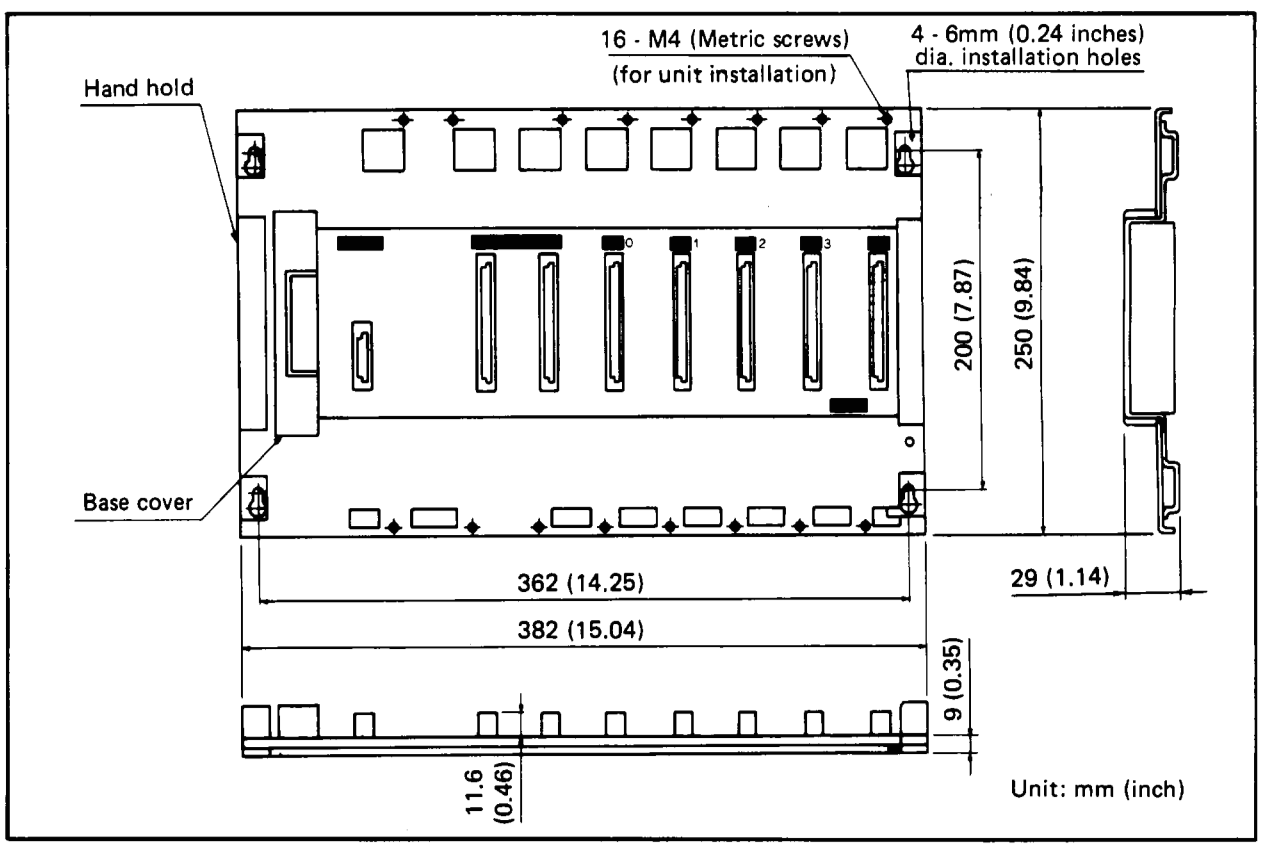
Unit: mm (inch)

3.4 Main base units

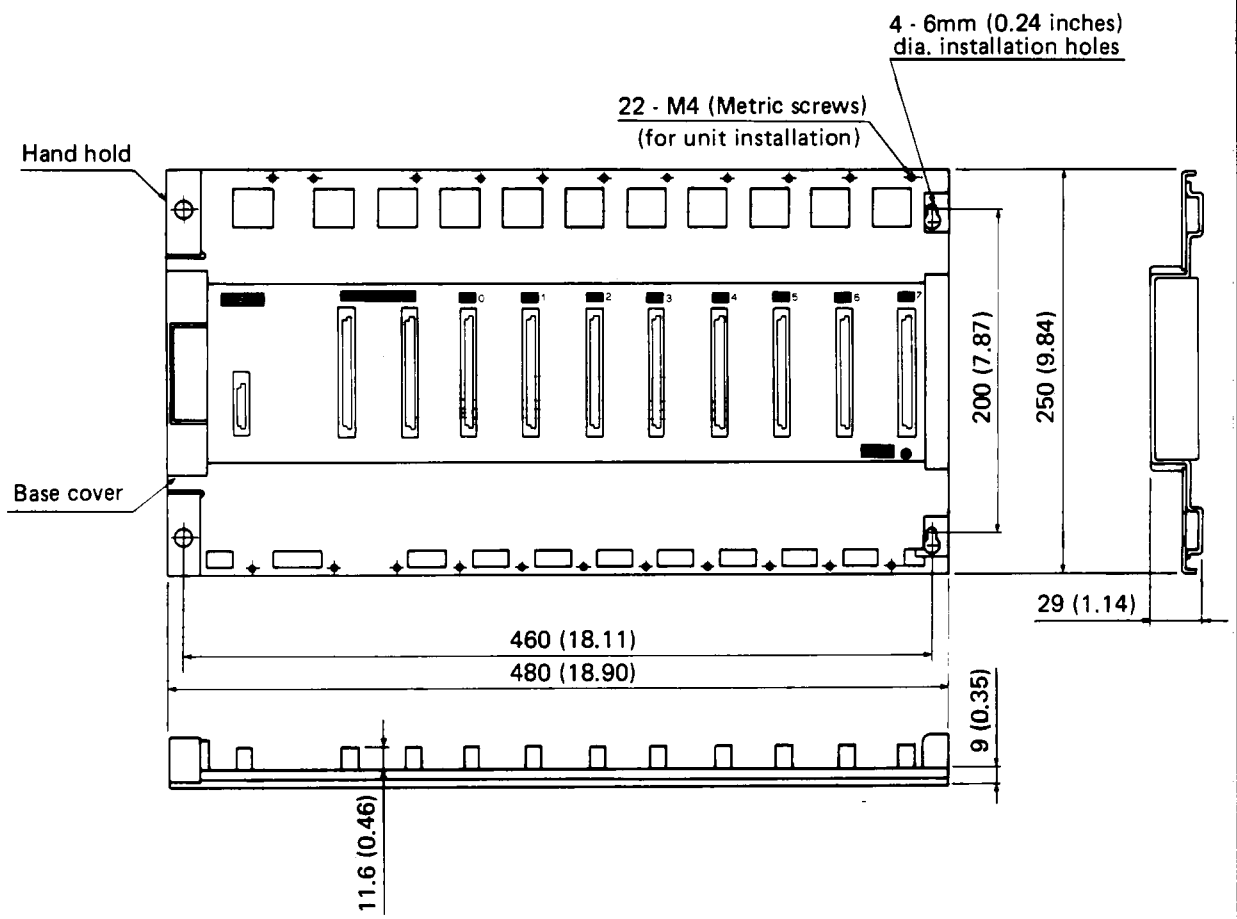
(1) Type A32B base unit



(2) Type A35B base unit



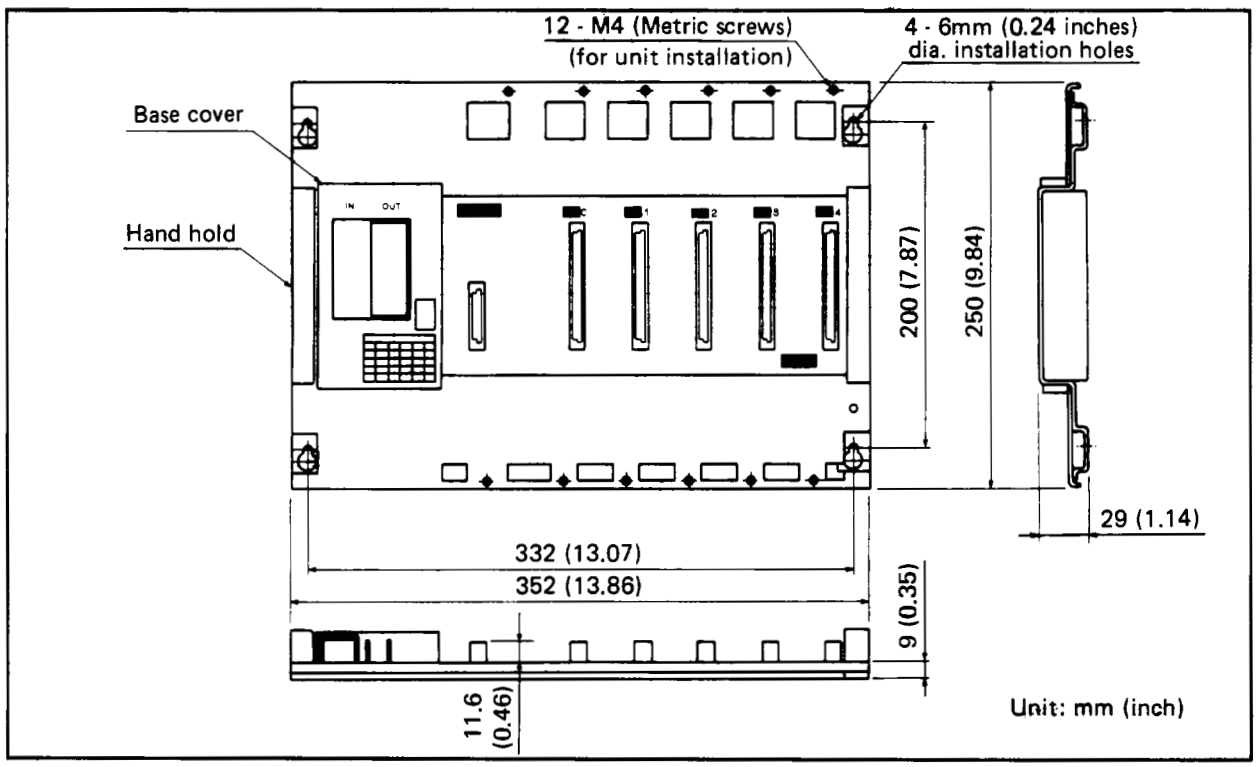
(3) Type A38B base unit



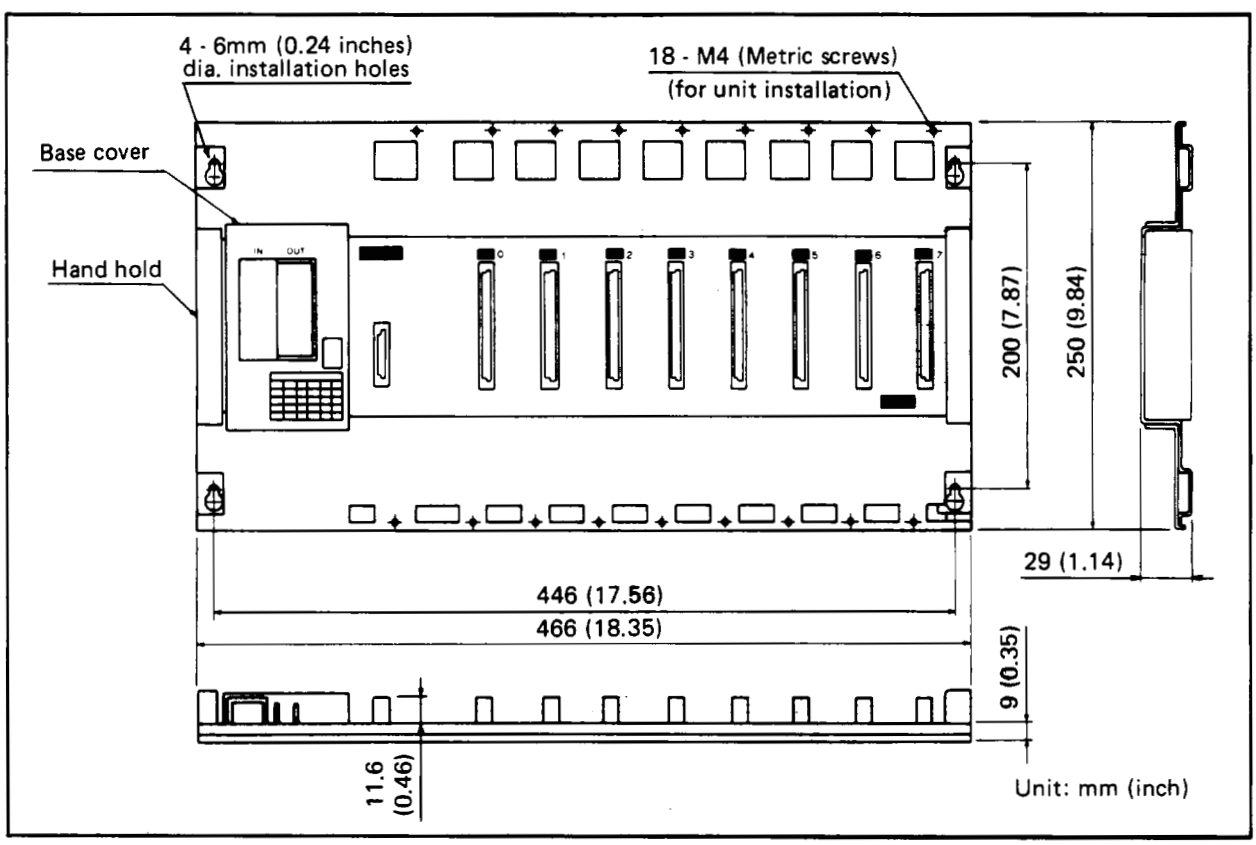
Unit: mm (inch)

3.5 Extension base units

(1) Type A65B base unit



(2) Type A68B base unit



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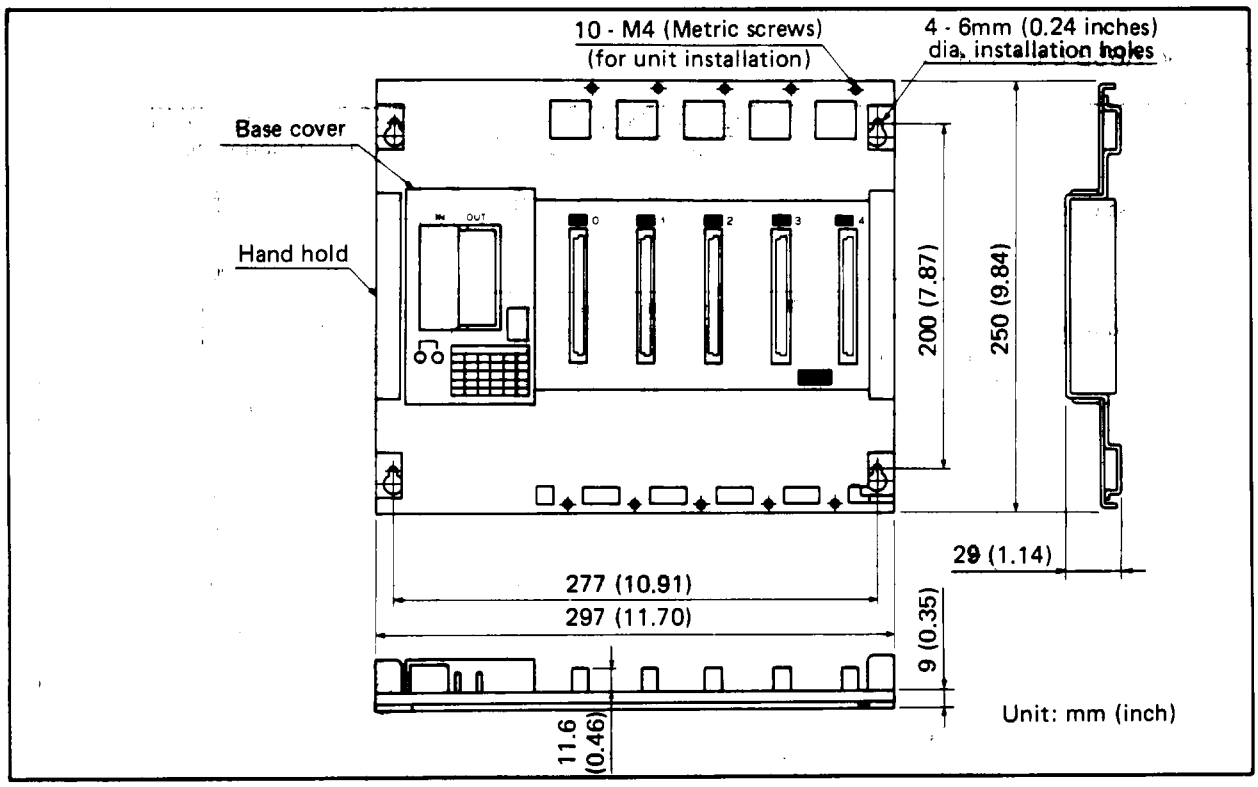
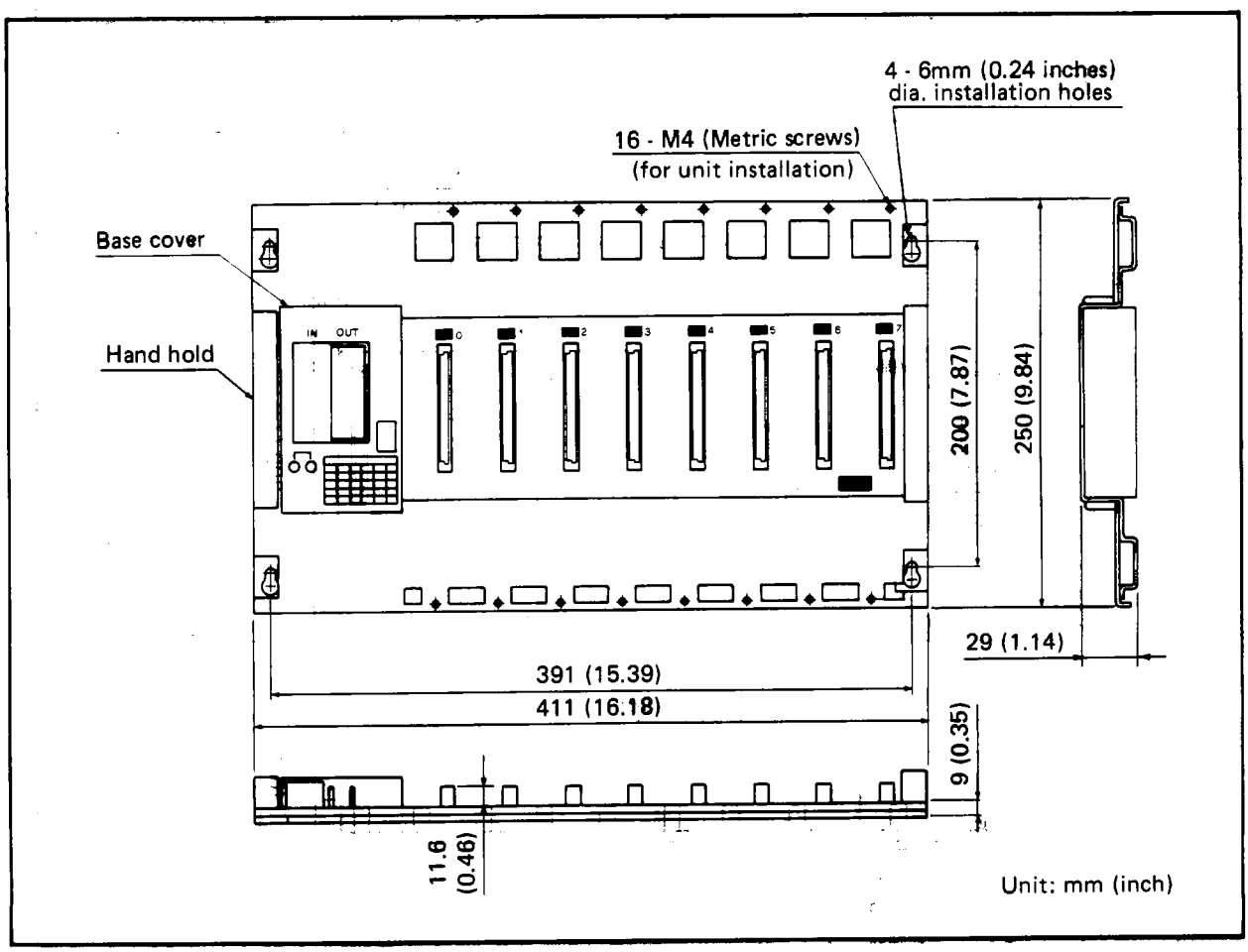
(3) Type A55B base unit



(4) Type A58B base unit



APPENDIX 4 Processing Time

The A3HCPU instruction processing times are give on the following pages.

(1) Processing time varies depending on the I/O control mode used with any instruction operating on inputs or outputs.

(2) The processing time for each instruction is shown for refresh mode.
The refresh processing time after END can be calculated as follows:

Sequence program processing time =
(instruction processing time) + (END processing time) + (refresh processing time)
Obtained from the list

END processing time = (END instruction processing time) + (T/C processing time at END)

Refresh processing time = (input + output points)/16 x 4.375 (μs)

REMARKS

For input and output points, see Section 3.2.9 (3).

(3) The basic and application instruction non execution (i.e. scan only) time is expressed as follows:

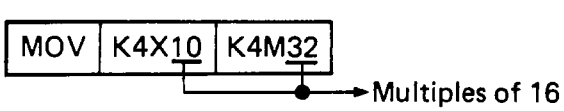
Unexecuted processing time = (instruction step number + 1) x 0.2 (μs)

(4) In the basic and application instruction processing time list, "Form A" and "Form B" are as described below:

Form A All of the following conditions are met:

1) Index qualification must not be specified.
2) File registers must not be used.
3) K4 or K8 must be specified as the device range when bit devices are used.
   K4 for 16-bit instruction
   K8 for 32-bit instruction
4) Device numbers specified as the head device of a series of bit devices must be a multiple of 16.

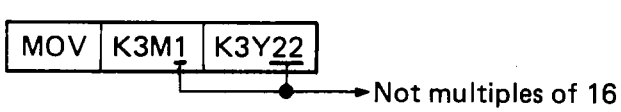
Example:



Form B Any of the following conditions is met:

1) Index qualification has been specified.
2) File registers are used.
3) K1 to K3 or K5 to K7 has been specified as the device range when bit devices are used.
4) Device numbers specified as the head device of a series of bit devices are not a multiple of 16.

Example:

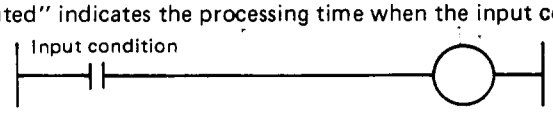


4.1 Sequence instructions

Instruction	Condition (Device)					Processing time (μsec)		Remarks
						Refresh mode	Direct mode	
LD LDI AND	X					0.2	2.0	
ANI OR ORI	Y, M, L, B, F, T, C					0.2		
ANB	———							
ORB	———							
OUT	Y	Unchanged (OFF → OFF, ON → ON)				0.35		
		Changed (OFF → ON, ON → OFF)				0.4	2.0	
	M (other than special M) L, B	Unchanged (OFF → OFF, ON → ON)				0.35		
		Changed (OFF → ON, ON → OFF)				0.4		
	Special M					1.4		
	F	Unexecuted				62		
		Executed				283		
	T	Instruction execution time				0.2		
		Processing time at END	Unexecuted			0		
			Executed	After time out		3.7		
				Added	K	5.9		
					D	6.5		
	C	Instruction execution time				0.2		"Uncounted" indicates that the counter does not count with the input condition remaining on.
		Processing time at END	Unexecuted			0		
			Executed	Uncounted		0		
				After count out		0		
				Counted	K	3.8		
					D	4.6		
SET	Y M L	Unexecuted				0.35		
		Executed	Unchanged (ON → ON)			0.35		
			Changed (OFF → ON)			0.4	2.0	
	Special M B	Unexecuted				0.8		
		Executed				1.4		
	F	Unexecuted				0.8		
		Executed				283		

REMARKS

"Unexecuted" indicates the processing time when the input condition is off.



Instruction	Condition (Device)			Processing time (μsec)		Remarks
				Refresh mode	Direct mode	
RST	Y M L	Unexecuted		0.35		
		Changed	Unchanged (ON → ON)	0.35		
			Changed (OFF → ON)	0.4	2.0	
	Special M B	Unexecuted		0.8		
		Executed		1.4		
	F	Unexecuted		0.8		
		Executed		427		
	T, C	Unexecuted		0.8		
		Executed		5.2		
	D, W, A, V, Z	Unexecuted		0.8		
		Executed				
	R	Unexecuted		0.8		
		Executed		56.5		
NOP	———			0.2		
END	M9084 off			1128		T/C and refresh processing times are not included.
	M9084 on			988		
MC	Y. M. L F. B	Unexecuted		2.6	6.4	
		Executed				
MCR	———			1.2		
PLS PLF	Y	Unexecuted		1.8	5.6	"Off" indicates that no pulse is generated with the input condition remaining on one scan after switched on (off for PLF).
		Executed	On			
			Off			
	M. L B. F	Unexecuted		1.8		
		Executed	On			
			Off			
SFT SFTP	Y	Unexecuted		0.8		
		Executed		10.9		
	M. L B. F	Unexecuted		0.8		
		Executed		10.9		
MPS	———			0.2		
MRD	———					
MPP	———					

4.2 Basic Instructions

4.2.1 Comparsion instructions

Instruction			Processing Time (μsec) Form A: Refresh mode: All devices	Form A: Direct mode: Other than X, Y	Form A: Direct mode: X,Y	Form B: Refresh mode: All devices	Form B: Direct mode: Other than X, Y	Form B: Direct mode: X,Y	Remarks
L D=	S1	S2	2.8	2.8	10.4	27.4	27.4	42.6	
A N D=	S1	S2	1.8	1.8	9.4	26.6	26.6	41.8	
O R=	S1	S2	3.2	3.2	10.8	27.8	27.8	43.0	
L D D=	S1	S2	157	157	180	212	212	235	
A N D D=	S1	S2	157	157	180	211	211	234	
O R D=	S1	S2	158	158	181	213	213	236	
L D< >	S1	S2	2.8	2.8	10.4	27.4	27.4	42.6	
A N D< >	S1	S2	1.8	1.8	9.4	26.6	26.6	41.8	
O R< >	S1	S2	3.2	3.2	10.8	27.8	27.8	43.0	
L D D< >	S1	S2	158	158	181	215	215	238	
A N D D< >	S1	S2	158	158	181	214	214	237	
O R D< >	S1	S2	161	161	184	216	216	239	
L D>	S1	S2	2.8	2.8	10.4	27.4	27.4	42.6	
A N D>	S1	S2	1.8	1.8	9.4	26.6	26.6	41.8	
O R>	S1	S2	3.2	3.2	10.8	27.8	27.8	43.0	
L D D>	S1	S2	158	158	181	216	216	239	
A N D D>	S1	S2	158	158	181	216	216	239	
O R D>	S1	S2	161	161	184	218	218	241	

Instruction			Processing Time (μsec)						Remarks
			Form A			Form B			
			Refresh mode	Direct mode		Refresh mode	Direct mode		
			All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
L D<=	S1	S2	2.8	2.8	10.4	27.4	27.4	42.6	
A N D<=	S1	S2	1.8	1.8	9.4	26.6	26.6	41.8	
O R<=	S1	S2	3.2	3.2	10.8	27.8	27.8	43.0	
L D D<=	S1	S2	158	158	181	216	216	239	
A N D D<=	S1	S2	158	158	182	215	215	238	
O R D<=	S1	S2	161	161	184	218	218	241	
L D<	S1	S2	2.8	2.8	10.4	27.4	27.4	42.6	
A N D<	S1	S2	1.8	1.8	9.4	26.6	26.6	41.8	
O R<	S1	S2	3.2	3.2	10.8	27.8	27.8	43.0	
L D D<	S1	S2	159	159	182	216	216	239	
A N D D<	S1	S2	158	158	181	216	216	239	
O R D<	S1	S2	160	160	183	217	217	240	
L D>=	S1	S2	2.8	2.8	10.4	27.4	27.4	42.6	
A N D>=	S1	S2	1.8	1.8	9.4	26.6	26.6	41.8	
O R>=	S1	S2	3.2	3.2	10.8	27.8	27.8	43.0	
L D D>=	S1	S2	160	160	183	216	216	239	
A N D D>=	S1	S2	158	158	181	215	215	238	
O R D>=	S1	S2	161	161	184	218	218	241	

4.2.2 BIN arithmetic operation instructions

Instruction				Processing Time (μsec) Form A Refresh mode All devices	Form A Direct mode Other than X, Y	Form A Direct mode X,Y	Form B Refresh mode All devices	Form B Direct mode Other than X, Y	Form B Direct mode X,Y	Remarks
+	S	D		1.6	1.6	9.2	41.6	41.6	56.8	
+P	S	D		1.6	1.6	9.2	41.6	41.6	56.8	
D+	S	D		3.0	3.0	18.2	50.2	50.2	73.0	
D+P	S	D		3.0	3.0	18.2	50.2	50.2	73.0	
+	S1	S2	D	1.8	1.8	13.2	41.6	41.6	64.4	
+P	S1	S2	D	1.8	1.8	13.2	41.6	41.6	64.4	
D+	S1	S2	D	3.0	3.0	25.8	50.0	50.0	84.2	
D+P	S1	S2	D	3.0	3.0	25.8	50.0	50.0	84.2	
−	S	D		1.6	1.6	9.2	41.6	41.6	56.8	
−P	S	D		1.6	1.6	9.2	41.6	41.6	56.8	
D−	S	D		3.0	3.0	18.2	50.2	50.2	73.0	
D−P	S	D		3.0	3.0	18.2	50.2	50.2	73.0	
−	S1	S2	D	1.8	1.8	13.2	41.6	41.6	64.4	
−P	S1	S2	D	1.8	1.8	13.2	41.6	41.6	64.4	
D−	S1	S2	D	3.0	3.0	25.8	50.0	50.0	84.2	
D−P	S1	S2	D	3.0	3.0	25.8	50.0	50.0	84.2	
✳	S1	S2	D	2.4	2.4	17.6	43.4	43.4	70.0	
✳P	S1	S2	D	2.4	2.4	17.6	43.4	43.4	70.0	
D✳	S1	S2	D	18.2	18.2	41	469	469	514	
D✳P	S1	S2	D	18.2	18.2	41	469	469	514	

Instruction				Processing Time (μsec) Form A Refresh mode All devices	Form A Direct mode Other than X, Y	Form A Direct mode X,Y	Form B Refresh mode All devices	Form B Direct mode Other than X, Y	Form B Direct mode X,Y	Remarks
／	S1	S2	D	8.6	8.6	20.0	47.6	47.6	70.4	
／P	S1	S2	D	8.6	8.6	20.0	47.6	47.6	70.4	
D／	S1	S2	D	36.8	36.8	59.6	493	493	538	
D／P	S1	S2	D	36.8	36.8	59.6	493	493	538	
I N C	D			1.2	1.2	5.0	27.8	27.8	35.4	
I N C P	D			1.2	1.2	5.0	27.8	27.8	35.4	
D I N C	D			2.2	2.2	9.8	33.8	33.8	45.2	
D I N C P	D			2.2	2.2	9.8	33.8	33.8	45.2	
D E C	D			1.2	1.2	5.0	27.8	27.8	35.4	
D E C P	D			1.2	1.2	5.0	27.8	27.8	35.4	
D D E C	D			2.2	2.2	9.8	33.8	33.8	45.2	
D D E C P	D			2.2	2.2	9.8	33.8	33.8	45.2	

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4.2.3 BCD arithmetic operation instructions

Instruction				Processing Time (μsec)						Remarks
				Form A			Form B			
				Refresh mode	Direct mode		Refresh mode	Direct mode		
				All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
B+	S	D		3.6	3.6	11.2	43	43	58.2	
B+P	S	D		3.6	3.6	11.2	43	43	58.2	
D B+	S	D		46.8	46.8	62	84	84	107	
D B+P	S	D		46.8	46.8	62	84	84	107	
B+	S1	S2	D	23.0	23.0	34.4	43	43	65.8	
B+P	S1	S2	D	23.0	23.0	34.4	43	43	65.8	
D B+	S1	S2	D	274	274	308	350	350	384	
D B+P	S1	S2	D	274	274	308	350	350	384	
B−	S	D		3.6	3.6	11.2	43	43	58.2	
B−P	S	D		3.6	3.6	11.2	43	43	58.2	
D B−	S	D		46.8	46.8	6.2	84	84	107	
D B−P	S	D		46.8	46.8	6.2	84	84	107	
B−	S1	S2	D	23.0	23.0	34.4	43.0	43.0	65.8	
B−P	S1	S2	D	23.0	23.0	34.4	43.0	43.0	65.8	
D B−	S1	S2	D	261	261	306	337	337	382	
D B−P	S1	S2	D	261	261	306	337	337	382	
B*	S1	S2	D	10.8	10.8	22.2	66.8	66.8	93.4	
B*P	S1	S2	D	10.8	10.8	22.2	66.8	66.8	93.4	
D B*	S1	S2	D	693	693	738	833	833	878	
D B*P	S1	S2	D	693	693	738	833	833	878	

Instruction				Processing Time (μsec) Form A Refresh mode All devices	Form A Direct mode Other than X, Y	Form A Direct mode X,Y	Form B Refresh mode All devices	Form B Direct mode Other than X, Y	Form B Direct mode X,Y	Remarks
B/	S1	S2	D	25.2	25.2	40.4	49	49	71.8	
B/P	S1	S2	D	25.2	25.2	40.4	49	49	71.8	
DB/	S1	S2	D	748	748	793	823	823	868	
DB/P	S1	S2	D	748	748	793	823	823	868	

4.2.4 BCD ⟷ BIN conversion instructions

Instruction			Processing Time (μsec) Form A Refresh mode All devices	Form A Direct mode Other than X, Y	Form A Direct mode X,Y	Form B Refresh mode All devices	Form B Direct mode Other than X, Y	Form B Direct mode X,Y	Remarks
B C D	S	D	1.6	1.6	9.2	28.4	28.4	43.6	
B C D P	S	D	1.6	1.6	9.2	28.4	28.4	43.6	
D B C D	S	D	9.4	9.4	24.6	59	59	81.8	
D B C D P	S	D	9.4	9.4	24.6	59	59	81.8	
B I N	S	D	1.6	1.6	9.2	28.4	28.4	43.6	
B I N P	S	D	1.6	1.6	9.2	28.4	28.4	43.6	
D B I N	S	D	3.6	3.6	18.8	59.2	59.2	82	
D B I N P	S	D	3.6	3.6	18.8	59.2	59.2	82	

4.2.5 Data transfer instructions

Instruction	Processing Time (μsec)						Remarks
	Form A			Form B			
	Refresh mode	Direct mode		Refresh mode	Direct mode		
	All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
MOV S D	1.2	1.2	8.8	27.6	27.6	42.8	
MOVP S D	1.2	1.2	8.8	27.6	27.6	42.8	
DMOV S D	2.0	2.0	17.2	33.0	33.0	55.8	
DMOVP S D	2.0	2.0	17.2	33.0	33.0	55.8	
XCH D1 D2	1.8	1.8	9.4	56.4	56.4	71.6	
XCHP D1 D2	1.8	1.8	9.4	56.4	56.4	71.6	
DXCH D1 D2	3.6	3.6	18.8	67.2	67.2	90.0	
DXCHP D1 D2	3.6	3.6	18.8	67.2	67.2	90.0	
CML S D	1.4	1.4	9.0	27.8	27.8	43.0	
CMLP S D	1.4	1.4	9.0	27.8	27.8	43.0	
DCML S D	2.6	2.6	17.8	49.4	49.4	72.2	
DCMLP S D	2.6	2.6	17.8	49.4	49.4	72.2	
BMOV S D n	132	132	862	5488	5488	6948	If n=96
BMOVP S D n	132	132	862	5488	5488	6948	If n=96
FMOV S D n	66	66	435	3873	3873	4238	If n=96
FMOVP S D n	66	66	435	3873	3873	4238	If n=96

4.2.6 Program branch instructions

Instruction \ I/O control mode	Processing Time (μsec) Refresh mode	Processing Time (μsec) Direct mode	Remarks
CJ P＊＊	4.0		Without index qualification
	7.2		With index qualification
SCJ P＊＊	4.0		Without index qualification
	7.2		With index qualification
JMP P＊＊	3.8		
※1 FEND	1128		M9084 off
	988		M9084 on
CALL P＊＊	8.2		Without index qualification
	11.8		With index qualification
CALLP P＊＊	8.2		Without index qualification
	11.8		With index qualification
RET	5.8		
IRET	61.6		
DI	52.5		
EI	53.0		
FOR n	5.8		
NEXT	6.4		
STOP	——		
※1 CHG	1128		M9084 off
	988		M9084 on
SUB n	86		Without index qualification
	88		With index qualification
SUBP n	86		Without index qualification
	88		With index qualification

POINT

FEND and CHG (marked ※1) do not include the T/C (at END) and refresh processing times.

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4.3 Application instructions

4.3.1 Display instructions

Instruction \ I/O control mode		Processing Time (μsec)		Remarks
		Refresh mode	Direct mode	
LED	S	282		
LEDC	S	320		
LEDA	ASCII characters	262		
LEDB	ASCII characters	262		
LEDR		460		

4.3.2 Logical operation instructions

Instruction	Processing Time (μsec)						Remarks
	Form A			Form B			
	Refresh mode	Direct mode		Refresh mode	Direct mode		
	All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
WAND S D	1.6	1.6	9.2	41.0	41.0	56.2	
WANDP S D	1.6	1.6	9.2	41.0	41.0	56.2	
DAND S D	27.4	27.4	42.6	49.8	49.8	72.6	
DANDP S D	27.4	27.4	42.6	49.8	49.8	72.6	
WAND S1 S2 D	20.8	20.8	32.2	40.8	40.8	63.6	
WANDP S1 S2 D	20.8	20.8	32.2	40.8	40.8	63.6	
WOR S D	1.6	1.6	9.2	41.0	41.0	56.2	
WORP S D	1.6	1.6	9.2	41.0	41.0	56.2	
DOR S D	27.4	27.4	42.6	49.8	49.8	72.6	
DORP S D	27.4	27.4	42.6	49.8	49.8	72.6	
WOR S1 S2 D	20.8	20.8	32.2	41.0	41.0	63.4	
WORP S1 S2 D	20.8	20.8	32.2	41.0	41.0	63.4	
WXOR S D	1.6	1.6	9.2	41.0	41.0	56.2	
WXORP S D	1.6	1.6	9.2	41.0	41.0	56.2	
DXOR S D	27.4	27.4	42.6	49.8	49.8	72.6	
DXORP S D	27.4	27.4	42.6	49.8	49.8	72.6	
WXOR S1 S2 D	20.8	20.8	32.2	41.0	41.0	63.4	
WXORP S1 S2 D	20.8	20.8	32.2	41.0	41.0	63.4	
WXNR S D	1.6	1.6	9.2	41.0	41.0	56.2	
WXNRP S D	1.6	1.6	9.2	41.0	41.0	56.2	

Instruction	Processing Time (μsec)						Remarks
	Form A			Form B			
	Refresh mode	Direct mode		Refresh mode	Direct mode		
	All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
DXNR S D	27.4	27.4	42.6	49.8	49.8	72.6	
DXNRP S D	27.4	27.4	42.6	49.8	49.8	72.6	
WXNR S1 S2 D	20.8	20.8	32.2	41.0	41.0	63.4	
WXNRP S1 S2 D	20.8	20.8	32.2	41.0	41.0	63.4	
NEG D	14.4	14.4	18.2	27.0	27.0	34.6	
NEGP D	14.4	14.4	18.2	27.0	27.0	34.6	

4.3.3 Rotation instructions

Instruction \ I/O control mode	Processing Time (μsec)		Remarks
	Refresh mode	Direct mode	
ROR n	4.8		Without index qualification
	5.6		With index qualification
RORP n	4.8		Without index qualification
	5.6		With index qualification
RCR n	6.8		Without index qualification
	7.6		With index qualification
RCRP n	6.8		Without index qualification
	7.6		With index qualification
ROL n	4.6		Without index qualification
	5.4		With index qualification
ROLP n	4.6		Without index qualification
	5.4		With index qualification
RCL n	6.8		Without index qualification
	7.6		With index qualification
RCLP n	6.8		Without index qualification
	7.6		With index qualification
DROR n	10.6		Without index qualification
	11.6		With index qualification
DRORP n	10.6		Without index qualification
	11.6		With index qualification
DRCR n	13.0		Without index qualification
	14.2		With index qualification
DRCRP n	13.0		Without index qualification
	14.2		With index qualification
DROL n	10.6		Without index qualification
	11.8		With index qualification
DROLP n	10.6		Without index qualification
	11.8		With index qualification

Instruction / I/O control mode	Processing Time (μsec)		Remarks
	Refresh mode	Direct mode	
DRCL n	13.0		Without index qualification
	14.2		With index qualification
DRCLP n	13.0		Without index qualification
	14.2		With index qualification

4.3.4 Shift instructions

Instruction	Processing Time (μsec)						Remarks
	Form A			Form B			
	Refresh mode	Direct mode		Refresh mode	Direct mode		
	All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
S F R D n	4.0	4.0	7.8	34.2	34.2	41.8	
S F R P D n	4.0	4.0	7.8	34.2	34.2	41.8	
B S F R D n	116	116	154	123	123	161	If n=5
	117	117	155	132	132	170	If n=15
B S F R P D n	116	116	154	123	123	161	If n=5
	117	117	155	132	132	170	If n=15
D S F R D n	15.2	15.2	—	134	134	—	If n=5
	27.2	27.2	—	141	141	—	If n=15
D S F R P D n	15.2	15.2	—	134	134	—	If n=5
	27.2	27.2	—	141	141	—	If n=15
S F L D n	4.0	4.0	7.8	34.4	34.4	42.0	
S F L P D n	4.0	4.0	7.8	34.4	34.4	42.0	
B S F L D n	116	116	154	123	123	166	If n=5
	117	117	155	132	132	175	If n=15
B S F L P D n	116	116	154	123	123	166	If n=5
	117	117	155	132	132	175	If n=15
D S F L D n	15.8	15.8	—	134	134	—	If n=5
	27.8	27.8	—	141	141	—	If n=15
D S F L P D n	15.8	15.8	—	134	134	—	If n=5
	27.8	27.8	—	141	141	—	If n=15

4.3.5 Data processing instructions

Instruction	Instruction form / I/O control mode / Device uses	Processing Time (μsec)						Remarks
		Form A			Form B			
		Refresh mode	Direct mode		Refresh mode	Direct mode		
		All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
SER S1 S2 n		187	187	—	191	191	—	If n=5
		260	260	—	264	264	—	If n=15
SERP S1 S2 n		187	187	—	191	191	—	If n=5
		260	260	—	264	264	—	If n=15
SUM S		14.4	14.4	18.2	26	26	33.6	
SUMP S		14.4	14.4	18.2	26	26	33.6	
DSUM S		33.8	33.8	37.6	41.2	41.2	52.6	
DSUMP S		33.8	33.8	37.6	41.2	41.2	52.6	
DECO S D n		200	200	205	216	216	221	If n=2
		240	240	307	267	267	328	If n=8
DECOP S D n		200	200	205	216	216	221	If n=2
		240	240	307	267	267	328	If n=8
SEG S D		3.4	3.4	11.0	197	197	205	
ENCO S D n		188	188	193	196	196	201	If n=2
		296	296	357	298	298	359	If n=8
ENCOP S D n		188	188	193	196	196	201	If n=2
		296	296	357	298	298	359	If n=8
BSET D n		5.0	5.0	—	9.4	9.4	—	If n=5
		5.0	5.0	—	9.4	9.4	—	If n=15
BSETP D n		5.0	5.0	—	9.4	9.4	—	If n=5
		5.0	5.0	—	9.4	9.4	—	If n=15
BRST D n		5.0	5.0	—	9.4	9.4	—	If n=5
		5.0	5.0	—	9.4	9.4	—	If n=15
BRSTP D n		5.0	5.0	—	9.4	9.4	—	If n=5
		5.0	5.0	—	9.4	9.4	—	If n=15

Instruction (Instruction form / I/O control mode / Device uses)	Processing Time (μsec)						Remarks
	Form A			Form B			
	Refresh mode	Direct mode		Refresh mode	Direct mode		
	All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
UNI S D n	145	145	—	148	148	—	If n=1
	155	155	—	158	158	—	If n=4
UNIP S D n	145	145	—	148	148	—	If n=1
	155	155	—	158	158	—	If n=4
DIS S D n	145	145	—	148	148	—	If n=1
	155	155	—	158	158	—	If n=4
DISP S D n	145	145	—	148	148	—	If n=1
	155	155	—	158	158	—	If n=4

4.3.6. FIFO instructions

Instruction			Processing Time (μsec)						Remarks
			Form A			Form B			
			Refresh mode	Direct mode		Refresh mode	Direct mode		
			All devices	Other than X, Y	X,Y	All devices	Other than X, Y	X,Y	
F I F W	S	D	136	136	140	143	143	151	
F I F W P	S	D	136	136	140	143	143	151	
F I F R	D1	D2	207	207	211	212	212	216	
F I F R	D1	D2	207	207	211	212	212	216	

4.3.7. ASCII conversion instructions

Instruction			Processing Time (μsec)		Remarks
			Refresh mode	Direct mode	
ASC	ASCII characters	D	107		

4.3.8 Special unit instructions

Instruction (I/O control mode)	Processing Time (μsec) Refresh mode	Processing Time (μsec) Direct mode	Remarks
FROM n1 n2 D n3	300		If n3=1
	5050		If n3=1000
FROMP n1 n2 D n3	300		If n3=1
	5050		If n3=1000
DFRO n1 n2 D n3	300		If n3=1
	5050		If n3=500
DFROP n1 n2 D n3	300		If n3=1
	5050		If n3=500
TO n1 n2 S n3	300		If n3=1
	5050		If n3=1000
TOP n1 n2 S n3	300		If n3=1
	5050		If n3=1000
DTO n1 n2 S n3	300		If n3=1
	5050		If n3=500
DTOP n1 n2 S n3	300		If n3=1
	5050		If n3=500
LRDP n1 S D n2	228		If n3=1
	228		If n3=32
LWTP n1 D S n2	236		If n3=1
	415		If n3=32
RFRP n1 n2 D n3	183		If n3=1
	183		If n3=32
RTOP n1 n2 D n3	185		If n3=1
	185		If n3=32

4.3.9 Other instructions

Instruction \ I/O control mode	Processing Time (μsec)		Remarks
	Refresh mode	Direct mode	
WDT	49.3		
WDTP	49.3		
CHK D1 D2	281.5		If the number of condition contacts is 1
	2210		If the number of condition contacts is 50
	4180		If the number of condition contacts is 100
	6140		If the number of condition contacts is 150
SLT	4100		If only device memory is latched
	10400		If device memory and R (8K points) are latched
SLTR	52.6		
STRA	51.8		
STRAR	51.8		
STC	1.2		
CLC	1.2		
DUTY n1 n2 D	121		
PR S D	183		
PRC S D	145		

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IMPORTANT

The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(1) Ground human body and work bench.

(2) Do not touch the conductive areas of the printed circuit board and its electrical parts with any non-grounded tools etc.

Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisty yourself as to its suitability for your specific application.

MITSUBISHI ELECTRIC CORPORATION

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